MV2 - MARVELL MV64560 implementation

This course covers Marvell Discovery V devices

Objectives

- The course describes the MV64560 internal data paths.
- The course explains how the host PowerPC and a CPU connected to PCI-X can synchronize to each other through the message unit.
- Operation of the PCI Express interface is detailed in Root Complex mode as well as in Endpoint mode.
- A long introduction to DDR SDRAM is done prior to describe the DDR SDRAM controller operation.
- The course focuses on the hardware implementation of the DDR SDRAM.
- The training explains how to implement chained DMA transfers, by using either IDMA channels or XOR engines.
- The course highlights the possible optimizations that can be implemented to boost the performance of the Ethernet controller.

- This course has been delivered several times to companies developing defence and avionics systems.

A more detailed course description is available on request at formation@ac6-formation.com

Pre-requisites

- Knowledge of PowerPC 60X / MPX bus. See our courses on NXP and IBM Microelectronics PowerPCs.

Related courses

- Ethernet and switching, reference cours N1 - Ethernet and switching
- PCI express, reference cours IC4 - PCI Express 3.0
- USB Full Speed High Speed and USB On-The-Go, reference cours IP2 - USB 2.0

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Plan du cours

OVERVIEW

- 5-bus architecture, organization of a board based on MV64560
- Frequency domains, fast path between CPU and SRAM / SDRAM
- Internal crossbar
- Master de-mux programming, address decode windows
- Slave mux programming, pizza arbiters operation
- Compatibility with MV64460

CPU INTERFACE

- CPU address space decoding
- Protection windows
- Arbitration, multi-processor operation
- CPU slave operation
- CPU master operation (60X mode)
- Cache coherency
- Deadlock avoidance

DDR1/2 INTERFACE

- Introduction to DDR SDRAM from Jedec specification
- Differences between DDR1 and DDR2
- DDR2 on-die terminations
- Initialization sequence
- DDR1/2 SDRAM controller
- Page management
- Transaction ordering
- Cache coherency
- ECC and read-modify-write transactions
- Low power modes

DEVICE CONTROLLER

- Functional description
- Address and data multiplexing
- Connecting 8/16 bit devices
- External acknowledgement
- Pack / unpack and burst support
- NAND flash support, boot from NAND flash

PCI INTERFACE

- PCI bus arbitration
- Master operation in PCI and PCI-X mode
- Target operation in PCI and PCI-X mode
- PCI-to-PCI configuration transactions
- Address decoding

PCI-EXPRESS x4 INTERFACE

- Integrated low power SERDES PHY

- x1, x4 link
- Operating as either Root Complex or Endpoint
- Link initialization
- Arbitration and ordering
- Messaging unit

GENERAL PURPOSE INPUT/ OUTPUT PINS

- GPIO port, functional description
- Interrupt request inputs
- Multi Purpose Pin multiplexing

INTERRUPT CONTROLLERS AND TIMERS

- Timers / counters
- Interrupt controller functional description
- Priority mechanism

TWSI CONTROLLER AND RESET

- I2C protocol basics
- TWSI controller functional description
- Master write sequence, master read sequence
- Slave write sequence, slave read sequence
- Reset pins and configuration
- Serial ROM initialization
- Requirement for an external Central Resource CPLD

IDMA CHANNELS

- IDMA address decoding
- Target unit and attributes programming
- Normal mode vs chained mode
- Transfer descriptors, descriptor ownership
- DMA interrupts

XOR ENGINES

- State machine : Active, Inactive and Paused states
- XOR operation mode
- CRC32 operation mode
- DMA operation mode
- Memory Initialization operation mode
- ECC error cleanup operation mode
- XOR Engines interrupts

16550 COMPATIBLE UARTs

- FIFO mode
- Flow control
- Transmit sequence
- Receive sequence

USB2.0 PORTS

- Address decoding
- Integrated PHY
- USB host operation, EHCI specification support

- USB device operation, Endpoint configuration

GIGABIT ETHERNET CONTROLLERS

- Interface to the PHY
- SGMII support
- Dedicated DMA
- Transmit weighted round-robin arbitration
- Backpressure mode
- Transmit and receive sequences
- Management interface
- Synchronous FIFO interface