# IC5 - RapidIO 3.0

*This course covers the RapidIO interconnect version 3.0*

## Objectives

- Packet switching benefits compared to shared busses are highlighted.
- The course explains the various traffic types that RapidIO supports: Input / output, Message and GSM.
- Mechanisms like error recovery and flow control are explained through various sequences.
- The course covers all features present in the RapidIO 3.0 specification, such as end-to-end flow control, multicast programming, data streaming and virtual output queuing extensions.
- CC-NUMA cache coherency mechanism is studied.
- The course describes the discovery sequence required to initialize the switches.
- Details of RapidIO interfaces present in NXP and IDT devices are provided to explain how theoretical statements are actually implemented .

A more detailed course description is available on request at training@ac6-training.com

## Prerequisites

- Experience of a digital bus such as PCI or Ethernet.

## Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

## Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

# Plan du cours

## THE TRANSITION TO PACKET SWITCHING

- Limitations of parallel shared buses
- Benefits of differential transmission
- Gigabit Serdes

## INTRODUCTION TO RAPIDIO

- Layer model, features of logical, transport and physical layers
- Packet encapsulation
- Purpose of control symbols
- Technical features: distributed memory vs message passing

## THE INPUT / OUTPUT LOGICAL TRAFFIC

- Accessing memory mapped address ranges
- Accessing the configuration space
- Atomic transactions
- Maintenance transaction
- Port write operation

## THE MESSAGE PASSING LOGICAL TRAFFIC

- Message vs doorbell
- Transmission of interrupts through doorbells, concept of virtual wires
- Management of messages split into several packets
- Detail of message passing implementation in NXP QorIQ devices

## CACHE COHERENCE

- Snooping basics
- GSM transactions, coherence domains
- The CC-NUMA approach
- Description of a directory entry: the sharing mask
- Analysis of various cache coherency sequences

## DATA STREAMING LOGICAL SPECIFICATION

- Mechanism of transporting an arbitrary protocol over a standard RAPIDIO interface
- Traffic streams
- Encapsulation methodology
- Support for PDU of 64 kB through segmentation and reassembly
- Class of services and virtual queues

## LOGICAL LAYER FLOW CONTROL

- Controlled flow list
- Watermarks setting
- XON-XOFF controls on transaction request flows
- Physical layer requirements
- Ordering rules

## THE TRANSPORT LAYER

- Packet routing through the network based on destination ID
- Programming interface to read / write the routing tables
- Multicast extensions
- Multicast mask and multicast group

## SYSTEM BRINGUP

- System exploration and initialization
- System enumeration API
- Hardware abstraction layer

## OVERVIEW OF THE PHYSICAL LAYER

- Packet acknowledgement
- Control symbols vs packet
- Multicast event

## ERROR MANAGEMENT

- Early processing of packets
- Study of various sequences explaining the ability of RAPIDIO to recover from errors automatically by hardware
- Port behaviour when error rate failed threshold is reached
- Drop packet enable
- Hot Swap Extensions
- Port behaviour when error rate failed threshold is reached
- Drop packet enable
- System software notification of errors

## PACKET PRIORITY AND FLOW CONTROL

- Mapping flowID into 2-bit priority
- Receiver based flow control, retry mechanism
- Transmitter based flow control, management of transmit credits
- Deadlock prevention

## THE LP-LVDS 8/16 INTERFACE (On request)

## THE LP-S 1x/4x INTERFACE

- Features or sublayers PCS and PMA
- Format of packets and symbols
- Single VC mode vs multiple VC mode, purpose of VC status control symbol
- The 8b/10b encoder / decoder
- Special characters, comma detection
- Lane synchronization
- 1.25Gbaud, 2.5Gbaud, and 3.125Gbaud LP-Serial Links
- 5Gbaud and 6.25Gbaud LP-Serial Links
- Transmit emphasis tuning
- Use of eye diagram to specify the electrical interface

## THE LP-S 1x/4x INTERFACE  10.3125 Gbaud OPERATION

- 64B/67B PCS and PMA Layers
- Scrambling
- Ordered sequences
- Electrical Specification for 10.3125 Gbaud LP-Serial Links
- Adaptive Equalization

## VIRTUAL OUTPUT QUEING EXTENSIONS

- Head Of Line blocking
- Congestion message
- Traffic staging
- Relationship with VC