FA1 - i.MX27 implementation + LTIB

This course describes the i.MX27 multimedia processor and Linux Target Image Builder tool

Objectives

- The course details the hardware implementation of the i.MX27 microcontroller.
- The boot sequence and the clocking are explained.
- The course explains all parameters that affect the performance of the system in order to easily perform the final tuning.
- A description of all internal peripherals is provided.
- An overview of the ARM926EJ-S core helps to understand issues caused by cache and MMU.
- The course ends with practical labs explaining how to generate a Linux image as well as a Root File System, by using a tool called LTIB [Linux Target Image Builder].

- This course has been delivered to several companies developing multimedia equipments.

A lot of programming examples have been developed by ACSYS to explain the boot sequence and the operation of complex peripherals.

- *They have been developed with GNU compiler and are executed under Lauterbach debugger.*
- *Furthermore, a host desktop running Fedora Linux is used to generate Linux image and Root File System during labs on LTIB.*

A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites

- This course provides an overview of the ARM926 core. Our course reference cours R1 - ARM7/9 implementationdetails the operation of this core.
- The following courses could be of interest:
  - USB Full Speed High Speed and USB On-The-Go, reference cours IP2 - USB 2.0
  - Ethernet and switching, reference cours N1 - Ethernet and switching

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Modalités d'évaluation

- Les prérequis indiqués ci-dessus sont évalués avant la formation par l'encadrement technique du stagiaire dans son entreprise, ou par le stagiaire lui-même dans le cas exceptionnel d'un stagiaire individuel.
- Les progrès des stagiaires sont évalués par des quizz proposés en fin des sections pour vérifier que les stagiaires ont assimilé les points présentés

- En fin de formation, une attestation et un certificat attestant que le stagiaire a suivi le cours avec succès.
  - En cas de problème dû à un manque de prérequis de la part du stagiaire, constaté lors de la formation, une formation différente ou complémentaire lui est proposée, en général pour conforter ses prérequis, en accord avec son responsable en entreprise le cas échéant.

Plan

ARCHITECTURE OF i.MX27

Overview

- ARM core based architecture
- Clarifying the internal data paths
- Highlighting the purpose of the 2 central interconnect units : MAX and M3IF
- Organization of a board based on i.MX27
- Mapping

CORE PLATFORM

THE ARM926EJ-S CORE

- Presentation of the core
- Operating modes
- Pipeline
- ARM vs Thumb instruction sets, interworking
- Branch instructions
- C-to-Assembly interface
- Exception mechanism
- Debug facilities

THE ARM9 PLATFORM

- AHB slave device latencies
- MAX parameterizing
- ARM Interrupt Controller [AITC]

HARDWARE IMPLEMENTATION

RESET AND CLOCKING

- Clock distribution
- Power-up sequence
- Low power modes, clock gating
- System boot mode selection
- Bootstrap mode operation

SYSTEM CONTROL

- GPIO module
- General Purpose Input interrupt request capability
- Signal description

ACCESSING EXTERNAL MEMORIES

- Description of the Master Arbitration and Buffering [MAB] unit

- Description of the M3IF arbitration [M3A]
- Enhanced DDR SDRAM controller
- NAND flash controller, boot from flash
- Programming the chip-selects

STANDARD PARALLEL INTERFACES

  - ATA controller
- PIO mode
- Ultra DMA mode
- FIFO receive and FIFO transmit alarms
  - MSHC
- Transfer protocol
- Error management
  - SDHC
- Interface to SD cards
- Transfer protocol
- Error management

MULTIMEDIA UNITS

DMA CONTROLLER

- Channel priority definition
- Burst length definition
- 2D memory transfers
- Double-buffering mechanism enabling chained transfers

VIDEO PROCESSING UNITS

  - Video acquisition
- CSI interface
- Configuring the interface to support CCIR656
  - Video pre-processor
- Image resizing
- Color space conversion
  - Video post-processor
- Deblock
- Dering
- Image resizing
- Color space conversion
  - Video codec
- MPEG-4 encoding / decoding
- H.264 AVC encoding / decoding

AUDIO RELATED INTERFACES

  - SSI interfaces
- Connection of Codecs or DSPs
- AC97 support
  - Digital audio multiplexor
- Connecting host interfaces to peripheral interfaces
- Internal network mode

SECURITY MODULES

  - Security Controller
  - SAHARA2 security coprocessor
- Random number generator

- Encryption / decryption sequences
  - Run-Time Integrity Checker
- SHA-1 message authentication
- Segmented data gathering
  - IC Identification Module

COMMUNICATION CONTROLLERS

  - 1-wire interface
  - Configurable SPI
- SPI protocol basics
- Master / slave operation
- Transfer sequence
  - I2C interfaces
- I2C protocol basics
- Master vs slave
- Transfer sequence
  - UART
- IrDA modulation / demodulation
- Support for Smart Card
- Flow control
  - USB
- Explaining what is OTG
- High-speed operation
- EHCI support
- Full speed operation
- Endpoint configuration
  - Fast Ethernet Controller [FEC]
- Buffer management, based on Buffer Descriptors
- Incoming frame filtering mechanisms
- VLAN support

LCD CONTROL

  - LCDC
- LCD screen format
- Standard panel interface for common LCD drivers
- Graphic window on screen
  - SLCDC
- Interface to an external display controller
- Transferring images and controls from DDR to the external controller

LTIB

GENERATING THE LINUX KERNEL IMAGE

- What is required on the host before installing LTIB
- Common package selection screen
- Common target system configuration screen
- Building a complete BSP with the default configurations
- Creating a Root Filesystems image
- Re-configuring the kernel under LTIB
- Selecting user-space packages
- Setup the bootloader arguments to use the exported RFS
- Debugging Uboot and the kernel by using Trace32
- Adding a new package
- Other deployment methods
- Creating a new package and integrating it into LTIB

Renseignements pratiques

Renseignements : 4 jours