# TK1 - KEYSTONE II IMPLEMENTATION

*This course covers all SoCs belonging to the KeyStone II, AM5K2E, 66AK2H and 66AK2E*

## OBJECTIVES

- The course details the hardware implementation of the Key Stone II.
- The course focuses on the boot sequence, the clocking and the power management strategies.
- The course explains all parameters that affect the performance of the system in order to easily perform the final tuning.
- The Ethernet MACs, as well as the Queue Manager and the Network Coprocessor are detailed.
- Interrupt management through ARM GIC is explained through a lab.
- The course also covers the hardware implementation, particularly the power supplies and the clocking
- All operation modes of EDMA3 are studied through use cases.
- General purpose high speed interfaces PCIe and USB3.0 are also handled.

A more detailed course description is available on request at training@ac6-training.com

### Prerequisites and related courses

- The Cortex-A15 ARM CPU is studied in a separate course.
  - See Cortex-A15 implementation and NEON programming RA3 - Cortex-A15 implementationcourse.
- The following courses could also be of interest:
  - PCIe IC4 - PCI Express 3.0course
  - Gigabit Ethernet N1 - Ethernet and switchingcourse
  - USB 3.0 IP3 - USB 3.0course

### Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

### Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

# Course Outline

## ARCHITECTURE OF KEY STONE II

- Describing the architectures of AM5K2E, 66AK2H, 66AK2E SoCs
- On-chip memories
- Clarifying the internal data paths: TeraNet masters and slaves
- Memory Protection Unit
- Organization of a board based on Key Stone II
- Summary of all peripheral features
- Memory mapping

## ARM COREPAC

- Cortex-A15 and integrated L2 cache instantiation options
- Integrated interrupt controller (GIC), detail of interrupt mapping
- Hardware big/little endian conversion
- Local Power and Sleep Controller
- Debug architecture
- Introduction to CoreSight, DAP features
- System Secure Controller SJC
- Embedded Trace Macrocell

## HARDWARE IMPLEMENTATION

- Power supplies, smart reflex
- Clock Control Module
- Reset Controller
- General Purpose Input/Output pins
- SerDes

## EDMA3 CONTROLLER

- DMA/QDMA Channel Logic
- Transfer controller, types of transfers
- Event queues
- Transfer Request Submission Logic
- Channel priority definition
- DMA/QDMA Channel Logic
- Parameter RAM (PaRAM):
- • Linking transfers
- • Channel controller shadow regions

## ACCESSING EXTERNAL MEMORIES

- DDR3 Controller
- EMIF16

## PCIe CONTROLLER

- Configuration as Agent or Root Complex
- Interrupt management, MSI
- Error management
- Configurable BAR filtering
- Inbound and outbound window programming
- Power management

## COMMUNICATION CONTROLLERS

- Enhanced CSPI
- I2C interfaces
- UART
- USB 3.0
- 1G/10G Ethernet Controller
- Ethernet switch
- Multicore Navigator
- Network coprocessor