



STR21 - STM32WL (Sub-GHz/LoRa)

This course describe the WL (Sub-GHz/LoRa) architecture and practical examples

Objectives

- Understand STM32WL SoC (Cortex-M4 + integrated Sub-GHz radio).
- Bring up CubeWL projects (SubGHz_Phy, LoRaWAN middleware).
- Configure RCC, RF clocks, SMPS/VDDPA, and RF paths.
- Build LoRa PHY links (SF/BW/CR, CAD, RX/TX).
- Deploy LoRaWAN Class A (OTAA/ABP), ADR, MAC cmds, downlinks.
- Apply low-power with radio; measure and tune current.
- Handle keys/NVM, region params, production RF checks.

Course Environment

- Theoretical course
 - PDF course material (in English) supplemented by a printed version for face-to-face courses.
 - Online courses are dispensed using the Teams video-conferencing system.
 - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- Practical activities
 - Practical activities represent from 40% to 50% of course duration.
 - Code examples, exercises and solutions
 - For remote trainings:
 - ▶ One Online Linux PC per trainee for the practical activities.
 - ▶ The trainer has access to trainees' Online PCs for technical and pedagogical assistance.
 - ▶ QEMU Emulated board or physical board connected to the online PC (depending on the course).
 - ▶ Some Labs may be completed between sessions and are checked by the trainer on the next session.
 - For face-to-face trainings:
 - ▶ One PC (Linux ou Windows) for the practical activities with, if appropriate, a target board.
 - ▶ One PC for two trainees when there are more than 6 trainees.
 - For onsite trainings:
 - ▶ An installation and test manual is provided to allow preinstallation of the needed software.
 - ▶ The trainer come with target boards if needed during the practical activities (and bring them back at the end of the course).
- Downloadable preconfigured virtual machine for post-course practical activities
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

Day 1

STM32WL SoC & radio overview

- Cortex-M4 core basics.
- Radio subsystem blocks.
- RFO_LP vs RFO_HP paths.
- SMPS / VDDPA roles.
- RF pins & routing.

Exercise: SoC & RF map

Project bring-up (CubeWL)

- Package structure (Drivers/MW).
- SubGHz_Phy vs LoRaWAN.
- Board/clock templates.
- Minimal UART/LED setup.
- Build & debug checks.

Exercise: App skeleton

RCC & RF clocking

- HSE/LSE choices.
- PLL to SYSCLK.
- RF timing sources.
- CCIPR selectors.
- MCO for verification.

Exercise: Clock profiles

RF front-end & power

- TX power config steps.
- RFO_LP/H Pout ranges.
- DC-DC vs LDO impact.
- Antenna match notes.
- PA ramp & duty cycle.

Exercise: TX power table

LoRa PHY basics

- SF / BW / CR fields.
- Preamble & sync word.
- CAD / RX timeout.
- Payload length limits.
- CRC/Invert IQ flags.

Exercise: PHY ping-pong

SUBGHZ driver & events

- Radio state machine.
- IRQs: TX done / RX done.
- Timeouts & errors.

- TX/RX scheduling.
- Simple CLI prints.

Exercise: Event logger

Day 2

LoRaWAN stack (Class A)

- Project layout (MW/LmHandler).
- Join flow OTAA.
- ABP fallback basics.
- RX1/RX2 windows.
- Confirmed vs unconfirmed.

Exercise: Join + uplink

Regions & channels

- EU868 vs US915 notes.
- Channels & sub-bands.
- Dwell time/duty cycle.
- LinkADRReq handling.
- Data rate plan.

Exercise: Region switch

ADR & downlinks

- ADR enable/disable.
- SNR/RSSI reporting.
- Rx win params tuning.
- Confirmed retry policy.
- App port mapping.

Exercise: Downlink LED

Security & keys

- Keys & key derivation.
- DevEUI policy (from UID).
- NVM/bond storage.
- Reset and rejoin rules.
- Basic key hygiene.

Exercise: Key store check

Sensors & payloads

- Simple sensor interface.
- Payload encode/FRMPayload.
- FPort selection.
- Uplink interval policy.
- Error counters.

Exercise: Temp uplink

Day 3

Low-power with radio

- Sleep/Stop policies.
- Radio sleep/standby.

- RTC tickless scheme.
- Wake sources & latency.
- Measurement method.

Exercise: LP profiles

Range & link budget

- RSSI/SNR basics.
- SF/BW impact.
- Antenna orientation.
- TX power vs battery.
- Simple path-loss model.

Exercise: Range walk

FSK mode (alt PHY)

- Freq dev & bit-rate.
- Preamble & filter.
- Packet format.
- CRC settings.
- Sensitivity trade-off.

Exercise: FSK ping

Downlink control & MAC cmds

- LinkADRReq/DevStatusReq.
- DutyCycleReq basics.
- RXParamSetupReq.
- NewChannelReq.
- Error handling.

Exercise: MAC trace

OTA/DFU workflow

- Boot/slots concept.
- Image versioning.
- Failure recovery.
- Rollback notes.
- Basic script use.

Exercise: App OTA (demo)

Production checklist (wrap-up)

- Region & channels fixed.
- TX power & duty policy.
- Keys/NVM procedure.
- RF test points noted.
- UID/serial/CRC tags.

Exercise: Self-audit