



SDR1 - DDR4 / LPDDR4

This course covers both DDR4 and LPDDR4 SDRAM

OBJECTIVES

- The course starts with a summary of DDR3/LPDDR3 specification.
- Then DDR4 functional description is studied.
- Differences between LPDDR4 and DDR4 are highlighted.
- ZQ calibration and write levelling sequences are detailed.
- The analog part is also described, particularly the tests to be performed using an oscilloscope.
- An example of DDR4 controller provides an example of programming interface.

A more detailed course description is available on request at training@ac6-training.com

PREREQUISITES

- Knowledge of SDRAM.

Course Environment

- Theoretical course
 - PDF course material (in English) supplemented by a printed version for face-to-face courses.
 - Online courses are dispensed using the Teams video-conferencing system.
 - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

DDR3 FUNCTIONAL DESCRIPTION

- DDR3 organization
- Burst chop mode
- Initialization sequence, new RESET# signal
- Dynamic ODT
- ZQ calibration
- Topologies, fly-by architecture
- Write leveling
- Low power modes

LPDDR3 FUNCTIONAL DESCRIPTION

- Power-up, initialization, and power-off
- Mode Register Read command
- Mode register definition

- Timings for Activate, Read, Write, Precharge
- Precharge & Auto Precharge clarification
- Refresh command
- Low power modes, self-refresh, partial array self refresh, power down, deep power down
- Temperature sensor
- CA training sequence
- ZQ calibration, write levelling

DDR4 FUNCTIONAL DESCRIPTION

- Bank group vs Bank address
- Alert output, CRC for write, Command Address parity
- Reset and initialization procedure
- Geardown mode
- BL8 burst order with CRC enabled
- Input clock frequency change
- Write levelling
- DQ training with MPR
- Temperature controlled refresh modes
- ZQ calibration
- Vref training
- Timings for Activate, Read, Write, Precharge
- Read preamble training
- Low power modes
- Connectivity test mode
- Pseudo-Open Drain termination

LPDDR4 FUNCTIONAL DESCRIPTION

- Pinout, addressing
- 2-channel architecture
- Power-up, initialization and power-off procedure
- Mode register definition
- Activation, read and write timing diagrams
- LPDDR4 Data Mask (DM) and Data Bus Inversion (DBI_{dc}) function
- Low power modes
- Vref training
- Frequency set point update timing
- Write levelling procedure
- Read DQ calibration
- ZQ calibration
- On-Die Termination

LPDDR4 ANALOG SPECIFICATION

- Differential Input Cross Point Voltage
- Slew rate requirements
- LVSTL(Low Voltage Swing Terminated Logic) IO System
- Temperature derating for AC timing
- CA Rx voltage and timing
- DQ Rx Voltage and Timing
- Using an oscilloscope to qualify the interface

DDR4 MEMORY CONTROLLER

- Example of NXP IP
- Address multiplexing: bank interleaving vs page interleaving
- PCB design considerations

- ECC implementation
- Tuning parameters
- Initiating write leveling, hardware vs software calibration
- Driver analog part configuration
- Memory testing