IN1 - Pentium-M implementation

This course covers Intel Pentium-M X86 low power processor

Objectives

- Optimized code writing based on pipeline knowledge.
- Data flows between SDRAM, L1 caches and L2 are explained.
- MESI cache coherency protocol is introduced in increasing depth.
- Vector instructions are viewed in detail.
- The course details the system startup sequence, particularly in multi-core platforms.
- The various modes of the memory management unit are described.

- This course has been delivered to several companies developing embedded systems.

A more detailed course description is available on request at formation@ac6-formation.com

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

INTRODUCTION TO PENTIUM-M

- Overview, implementation of IA-32 architecture
- Operation modes
- X86 fundamentals

REAL MODE

- Privilege levels
- Segments
- Accessing High Memory Area
- Flat mode

PROTECTED MODE

- Virtual memory
- X86 virtual mode
- Task management
- Segment descriptors : GDT vs LDT
- Code segment, conforming vs non-conforming segments

- Call gate utilization
- Data segment

MULTITASK HARDWARE MECHANISMS

- Task State Segment [TSS]
- Task gate
- Task switching
- I/O space protection

PAGE TRANSLATION

- 386 page translation
- PDE and PTE format
- Privilege level checking
- Pentium 4-MB pages
- PAE-36
- PSE-36

VIRTUAL MODE X86

- VMM requirements
- Video frame buffer virtualization

MEMORY TYPES

- Memory Type and Range Registers
- Page attribute table

EXCEPTION MANAGEMENT

- Vector table
- Priority between exceptions
- Exception management in real mode
- Exception management in protected mode
- Interrupt and trap gates
- Exception return
- Exception management in VM86 mode
- Acceleration mechanisms : sysenter and sysexit instructions

LOCAL APIC

- Interrupt management in SMP platforms
- Local interrupts
- Interrupt management sequence
- IPI generation and reception
- Message Signaled Interrupts
- MSI utilization in Pentium platforms

POWER MANAGEMENT

- Pentium-II power management, state machine
- Pentium-M power management, deeper sleep new state
- SpeedStep technology
- System Management Mode
- Interrupt management when SMM is active
- Transition to Power-Down

SYSTEM STARTUP

- Hardware configuration
- Processor state after a reset
- Selecting the bootstrap processor
- Configuring Auxiliary processors
- Microcode update

INSTRUCTION PIPELINE

- Detail of the 11 stages
- Hyper-threading, Pentium-4 implementation
- CPU resource utilization
- Instruction execution steps

CACHES

- L2 cache organization
- Hit under miss
- Miss under miss
- Squashing

PROGRAMMING

- Mixing 16-bit and 32-bit codes
- I/O space access instructions
- Addressing modes
- SSE instructions, register set