



IC7 - VME

This course covers VME bus, including 2eSST

Objectives

- This course is based on the ANSI-VITA 1 1994 specification and ANSI-VITA 1.1 extensions.
- The new 2eSST protocol is also described.
- The training highlights synchronization methods like mailbox generally used in VME based calculators.
- The daisy-chain acknowledge mechanism is viewed in detail.
- Shared resource management is also emphasized.
- The training shows how to configure a VME backplane.
- After having reminded the 68K interrupt management, the VME priority interrupt bus is described.
- VME timing diagrams are studied with the assistance of the VSYSTEMS analyser board.
- The course focuses on the configuration space specified in the VME64 and VME64x standards.
- This course has been delivered several times to companies developing defence and avionics equipments.

A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites

- Experience of a parallel digital bus is recommended.

Course Environment

- Theoretical course
 - PDF course material (in English) supplemented by a printed version for face-to-face courses.
 - Online courses are dispensed using the Teams video-conferencing system.
 - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

INTRODUCTION TO THE VME BUS

- VME based calculator architecture
- Connectors pinout
- The four bus parts

THE ARBITRATION BUS

- Explanation of the daisy-chain acknowledge mechanism
- RRS, PRI and ONE Arbiter options
- RWD, ROR, FAIR requester options
- Arbitration sequence analysis

THE DATA TRANSFER BUS

- Byte locations accessed during a data transfer
- Address pipelining
- Burst transfers
- Address Only transactions
- BTO timer utility
- Shared resource management

THE INTERRUPT BUS

- Interrupt generator structure
- Interrupt handler structure
- Status/ID read cycle
- ROAK and RORA interrupt generator options

THE UTILITY BUS

- SYSFAIL management
- Reset timing diagram
- Power control
- Auto system controller

ELECTRICAL SPECIFICATION

- The 5 signal types
- Bus driving and receiving requirements
- Noise margins
- Board powering, current ratings for power pins
- Line terminations
- The ETL transceiver logic required for 2eSST

THE CONFIGURATION SPACE

- Determination of the mapping of the A24 config space
- Detail of the CR and CSRs
- Auto slot ID mechanism

VME64x EXTENSIONS

- New P0/J0 connector
- P1/J1, P2/J2 connectors pinouts, rows z and d pin assignments
- Live insertion support
- EMC front panel and subracks
- ESD protection
- ETL technology
- 2eVME protocol

2eSST PROTOCOL

- 3U and 6U implementations
- Broadcast transfers
- Source synchronous transfers, data centered strobes
- Skew calculation