HX3 - Xilinx - Designing with Ethernet MAC logicores

This course covers the implementation of the Ethernet MAC Xilinx logicores.

Objectives

- Utilize various Ethernet cores, used either in standalone mode or as a peripheral in a processor-based design.
- Determine the appropriate core to use.
- Develop software to drive the core and achieve desired functionality.
- Integrate hard and soft IP into the EDK.

- This course is delivered by Ac6 engineers, expert of Gigabit Ethernet, who has developed trainings on 802.3 / 802.1 specification and Gigabit Ethernet implementation in AMCC, Intel, NXP processors and Marvell switches.

Xilinx software (ISE) is used to synthesize and implement practical examples, Mentor Graphics ModelSim is used for simulation.
A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites

- Knowledge of Ethernet is recommended, see our course reference N1.
- Experience with Xilinx ISE and EDK software tools is recommended.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

DAY 1

- Ethernet basics
- Network protocols
  - Lab1 : Analyzing Ethernet frames
- Physical layer
- Local Link interface
  - Lab2 : VLAN and Jumbo frames
- Xilinx EMAC solutions

DAY 2

  - Lab3 : Implementation
- EMAC and EMAC lite

    - Lab4 : EMAC peripheral in loopback mode
- GEMAC
- TEMAC
    - Lab5 : TEMAC in loopback mode
- 10GE MAC
    - Lab6 : Analyzing 10GE MAC frames