FF5 - MCF5225X implementation + MQX

This course covers MCF5225X ColdFire MCUs, for instance the MCF52259

OBJECTIVES

- Courses detail the hardware implementation of the MCF5225x MCU.
- Courses focuse on low level programming of the ColdFire V2 core.
- The training helps become familiar with CodeWarrior IDE.
- Practical exemples of internal software drivers are provided.
- More detailed course description available on request at formation@ac6-formation.com

New: *** Write your First NXP MQX" RTOS application ***

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.

Related courses

- Ethernet and switching, reference N1 - Ethernet and switchingcourse
- USB 2.0, reference IP2 - USB 2.0course
- CAN bus, reference IA1 - CAN buscourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- Practical activities
  - Practical activities represent from 40% to 50% of course duration.
  - Code examples, exercises and solutions
  - For remote trainings:
    - One Online Linux PC per trainee for the practical activities.
    - The trainer has access to trainees' Online PCs for technical and pedagogical assistance.
    - QEMU Emulated board or physical board connected to the online PC (depending on the course).
    - Some Labs may be completed between sessions and are checked by the trainer on the next session.
  - For face-to-face trainings:
    - One PC (Linux ou Windows) for the practical activities with, if appropriate, a target board.
    - One PC for two trainees when there are more than 6 trainees.
  - For onsite trainings:
    - An installation and test manual is provided to allow preinstallation of the needed software.
    - The trainer come with target boards if needed during the practical activities (and bring them back at the end of the course).
- Downloadable preconfigured virtual machine for post-course practical activities
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

INTRODUCTION TO MCF52259

Overview

- Coldfire roadmap
- MCF52259 umbrella device
- 5225X block diagram
- Pinout
- Memory mapped I/O organization

CORE ARCHITECTURE

- V2 pipeline
- Addressing modes
- Branch, data transfer, arithmetic, logic, shift & rotate, bit instructions
- Mac instructions
- C to assembly interface
- Section definition, parameterizing the linker command file
- Exception management
- Internal SRAM
- 5225X cache operation
- Power management

DEBUG FACILITIES

- Intrusive vs non-intrusive debug
- BDM port
- Hardware breakpoints
- Trace port

PLATFORM

RESET

- Reset sources
- Clocking
- Reset control flow
- Chip Configuration Module [CCM]
- Requirements of the boot routine

SYSTEM PERIPHERALS

- SCM
- The interrupt controller
- The Edge Port Module
- Watchdog timer module
- Programmable Interrupt Timer Modules

THE DMA CONTROLLER

- Channel prioritization
- Bandwidth control

- Transfer termination
- Utilization of DMA timers

HARDWARE IMPLEMENTATION

- Dynamic bus sizing
- Address decoding
- Data transfer sequence
- Burst cycles

MEMORY

- The Flash memory controller
- The SRAM
- The Mini-FlexBus

INTEGRATED I/Os

COMMUNICATION CONTROLLERS

- The UART Module
- The QSPI
- The I2C controller
- The FlexCAN controller
- The USB OTG controller
- The Fast Ethernet Controller

Exercise: With NXP MQX" software solutions

CRYPTOGRAPHY

- Cryptographic Acceleration Unit (CAU)
- Random Number Generator (RNG)