FD1 - DSP568XX implementation

This course covers the 568XX 16-bit DSP NXP family

Objectives

- The course explains how to design a 56807 based board.
- Optimized coding examples are described.
- A generic interrupt handler is introduced.
- The course focuses on motor driving.
- Practical exercices are executed on a 56807 board.

- This course has been delivered several times to companies developing electric engines.

A lot of programming examples have been developed by ACSYS to explain how to write optimized code.
• They have been developed with CodeWarrior compiler and are executed under CodeWarrior debugger.
A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites

- Basic knowledge about signal processing and motor control.
- Knowledge of CAN bus is recommended, see our course reference CAN bus, reference IA1 - CAN buscourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

INTRODUCTION TO DIGITAL SIGNAL PROCESSING

- Arithmetic processing of real-time signals
- Filtering, convolution, correlation
- Modified dual Harvard architecture
- DSP 568XX family introduction, compatibility with 5600X DSPs
- Introduction of motor types

568XX ARCHITECTURE

- Core buses
- Processing states
- Reset, low voltage, stop and wait operations

- 56807 mapping

THE DSP CORE

- The Data ALU
- The Address Generation Unit
- The Program Control Unit
- The instruction set
- C-to-assembly interface
- Software techniques
- Exception management
- The interrupt routing performed by the ICTN
- The debugging support
- JTAG use to access the OnCE
- The embedded flash memory
- Program sequence
- Erase sequence

HARDWARE IMPLEMENTATION

- On chip clock synthesis
- Wait state X data memory
- Wait state program memory

THE QUAD TIMER MODULE

- Timer module pinout
- Operating modes
- OFLAG output signal

THE ADCs

- Timing, pipelining
- Conversion sequence definition
- Synchronization to the PWM
- Optional sample correction

THE QUADRATURE DECODERS

- Quadrature decoders pinout
- Configurable digital filters
- Watchdog timer implementation

THE PULSE WIDTH MODULATORS

- Independent or complementary channel operation
- Deadtime generators
- IFault protection

THE SCI AND THE SPI MODULES

- SCI block diagram, IO signals
- Asynchronous vs synchronous operation modes
- Baud rate selection
- Bootstrap loading from the SCI
- Asynchronous transmit and receive sequences
- SPI synchronous communications basics
- Master vs slave selection

- Polarity selection

THE MSCAN CONTROLLER

- The MSCAN controllers
- Message buffers structure
- ID bit masking
- Arbitration
- Timing and synchronization
- Error management