FCQ8 - T1024 QorIQ implementation

This course covers NXP QorIQs T1024 & T1014

Objectives

- This course has the following objectives:
  - Describing the hardware implementation, particularly the boot sequence and the DDR3 controller
  - Understanding the features of the internal interconnect and related units and mechanisms such as PAMU, CPC and stashing
  - Explaining the standard bus interface controllers, PCIe, USB, SATA and MMC-SD
  - Describing the units which are interconnected to other modules, such as clocking, interrupt controller and DMA controller, because the boot program generally has to modify the setting of these units
  - Clarifying the operation of the Datapath Acceleration Architecture that assists the processor core in taking in charge buffer allocation, queue management, frame management and particularly incoming frame classification, pattern searching, and encryption
  - Describing the various debug units and their utilization to fix errors in a multicore / multimaster SoC.

A more detailed course description is available on request at training@ac6-training.com
This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Pre-requisites and related courses

- Experience of a 32-bit processor or DSP is mandatory.
- Note that the e5500 Power core is covered in a separate course reference FCC2 - e5500 implementationcourse.
- The following courses could also be useful:
  - PCIe IC4 - PCI Express 3.0course
  - Ethernet N1 - Ethernet and switchingcourse
  - USB 2.0 IP2 - USB 2.0course
  - SATA IS3 - Serial ATA IIIcourse
  - DDR4 SDR1 - DDR4 / LPDDR4course

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

T1024 ARCHITECTURE

OVERVIEW

- CoreNet coherency fabric
- Coherency subdomains
- Memory map, local access windows
- Highlighting data paths inside the T1024
- Application examples

SOC PLATFORM

POWER, RESET AND CLOCKING

- Reset causes
- Reset configuration words source
- Pre-boot loader
- PCIe configuration
- Clocking, system clock domains
- SerDes high speed lanes configuration
- Advanced power management

SECURE BOOT

- Internal boot ROM, secure boot sequence
- Security fuse processor
- Code signing
- External tamper detection
- Run time integrity checker
- Secure debug controller

CORENET PLATFORM CACHE

- Cache operation, write-through or write-back operation
- Operation as memory-mapped SRAM
- Partitioning between coherency domains
- Stashing, address-based or CoreNet signalled
- Soft error detection and correction

PERIPHERAL ACCESS MANAGEMENT UNIT (PAMU)

- Controlling master access permissions through Logical I/O Device Number
- Address translation
- Data structures, Peripheral Access Authorization and Control Entry
- Operation mode translation
- Steps in processing of DSA operations by PAMU
- PAMU gate closed state

IO BRIDGE

- Bridging agent
- Transaction ordering

- Resolution of coherency effects
- Authorization, access control and address mapping of I/O-initiated transactions flowing into the CoreNet coherency domain

MULTIPROCESSOR PERIPHERAL INTERRUPT CONTROLLER

- Open PIC architecture compatibility
- Interrupt nesting
- Message interrupts
- e5500-to-e5500 interrupt capability

LOW SPEED PERIPHERALS

- Description of the NS16452/16552 compliant Uarts
- I2C protocol fundamentals: addressing, multimaster operation
- Transfer timing diagrams, SCL and SDA pins
- eSPI controller

ENHANCED SDHC

- Interface to SD and MMC cards
- Transfer protocol, single block, multiple block read and write
- Internal and external DMA capabilities
- SD protocol unit

USB CONTROLLERS

- Host or device support
- High-speed operation
- EHCI support, scheduling the various transactions into frames
- Endpoint configuration
- Device operation

HARDWARE IMPLEMENTATION

THE DDR3 / 4 MEMORY CONTROLLER

- On-Die termination and calibration
- DDR3 fly-by architecture, write leveling
- Reset sequence, dynamic ODT, ZQ calibration
- Bank activation, read, write and precharge timing diagrams, page mode
- Initial configuration following Power-on-Reset
- Address decode unit
- Timing parameters programming
- Initialization routine
- Testing the memory using patterns

INTEGRATED FLASH CONTROLLER

- Functional muxing of pins between NAND, NOR, and GPCM
- Normal GPCM FSM
- Flexible timing control
- NOR flash FSM
- Configurable even/odd parity on address/data bus supported
- NAND flash FSM
- ONFI-2.0 asynchronous interface
- ECC generation/checking

- SLC and MLC Flash devices support with configurable page

INTEGRATED DMA CONTROLLERS

- Scatter / gathering
- Selectable hardware enforced coherency
- Ability to start DMA from external 3-pin interface

PCI EXPRESS INTERFACE

- Modes of operation, Root Complex / Endpoint
- Transaction ordering rules
- Programming inbound and outbound ATMUs
- Benefits of MSIs
- Low power management
- Configuration, initialization

SATA CONTROLLER

- Support for SATA II extensions
- Native command queuing, command descriptor
- Standard ATA master-only emulation
- Interrupt coalescing

DISPLAY INTERFACE UNIT

- Modes of operation
- Area descriptor
- Pixel structure
- Alpha-blending
- Chroma keying
- Gamma correction
- Internal DMA channels

DATAPATH PROCESSING SUBSYSTEM

DPAA OVERVIEW

- Data formats
- Frame formats
- Packet walk through
- DPAA Configuration and initialization

QUEUE MANAGER

- Objectives if this accelerator
- Structure of frame queues
- Active and suspended frame queues
- Frame queue descriptor, frame queue descriptor cache
- Frame queue state machine
- Work queues and channels
- Enqueue and dequeue portals
- Utilization of rings
- Dequeue dispatcher operation
- Message ring
- Congestion avoidance, Weighted Random Early Discard
- Order definition point implementation

BUFFER MANAGER

- Objectives if this accelerator
- Central resource pool management function
- Per-pool stockpile
- CoreNET software portals
- Direct connect portals
- Buffer Pool State Change Notifications

FRAME MANAGER

- Objectives if this accelerator
- FMAN submodules
- Rx BMI features
- Tx BMI features
- Offline parsing, host command features
- Frame processing manager
- FMan controller
- Parser
- Key generator
- Policer

DATA PATH THREE-SPEED ETHERNET CONTROLLERS

- Frame format with and without VLAN option
- Connection to packet FIFO interface
- Physical interfaces
- 256-entry hash table for unicast and multicast
- Accessing PHY registers
- RMON statistic counters, carry registers
- Client IEEE1588 timers

10-GIGABIT MAC

- XAUI interface to PHY
- Multicast address filtering
- Dynamic inter packet gap (IPG) calculation
- MAC address insertion
- Support for VLAN
- IEEE 1588 timestamping

SECURITY ENGINE

- Introduction to DES, 3DES and AES algorithms
- Job management using QMan interface
- Input / output rings
- Cryptographic operations
- Data movement, FIFOs
- Scatter / gather DMA
- Selecting the authentication / cryptographic algorithm
- Run Time Integrity Checking
- Example, implementing IPSec

GLOBAL FUNCTIONS, DEVELOPMENT AND DEBUG

PERFORMANCE MONITOR AND DEBUG FEATURES

- Introduction to NEXUS specification
- NEXUS Aurora link
- Event processing unit
- Watchpoint facility
- Trace buffer
- Event Combining for the Creation of Advanced Triggers
- Cross-Functional Debug Components
- DDR SDRAM interface debug, measuring per-master bandwidth

QUICC ENGINE

OVERVIEW OF QUICC ENGINE

- Integrated RISC CPU
- Communication between Host CPU and QE RISC CPU

INTEGRATED INTERRUPT CONTROLLER

- Priority management
- Steering the interrupt source to either Low priority or High priority input of the platform PIC

SYSTEM INTERFACE AND CONNECTION TO EXTERNAL COMMUNICATION PORTS

- Serial DMA
- QUICC engine external requests
- NMSI vs TDM
- Enabling connections to TSA or NMSI

BUFFER MANAGEMENT

- Utilization of Buffer Descriptors
- Chaining descriptors into rings
- Parameter RAM independent of protocol

UNIFIED COMMUNICATION CONTROLLERS

- UCC as slow communications controllers, UART mode
- UCC for fast protocols, virtual FIFOs

UCC HDLC CONTROLLER

- Flow control
- Setting global parameters
- Describing the parameter RAM

UCC TRANSPARENT CONTROLLER

- Transparent data encapsulation, frame sync and frame CRC
- Describing the parameter RAM

SERIAL INTERFACE

- Connecting TDM lines
- Parameterizing the timings related to Rx/Tx clock, sync and data signals
- Connecting the TDM line to UCC using Rx/Tx routing tables

MULTI-CHANNEL CONTROLLER ON UCC - UMCC

- Comparison with MCC and QMC
- Connecting time-slots to logical channels through Rx/Tx routing tables
- Implementing Rx/Tx channel buffers
- Interrupt management
- Channel-specific HDLC parameters
- Per channel exception management
- UMCC host commands