STR4 - STM32 F0-Series implementation

This course covers STM32F050 and STM32F051 ARM-based MCU family

Objectives

- This course has 5 main objectives:
  - Describing the hardware implementation and highlighting the pitfalls
  - Describing the ARM Cortex-M0 core architecture
  - Becoming familiar with the IDE and low level programming
  - Describing the units which are interconnected to other modules, such as clocking, interrupt controller and DMA controller, because the boot program generally has to modify the setting of these units
  - Describing independent I/O modules and their drivers.
- Note that this course has been designed from the architecture of the most complex STM32 F1-Series device, the STM32F051.
- Consequently, a chapter has been designed by Acsys for each possible integrated IP.
  - According to the actual reference chosen by the customer, some chapters may be removed.
- Products and services offered by ACSYS:
  - ACSYS is able to assist the customer by providing consultancies. Typical expertises are done during board bringup, hardware schematics review, software debugging, performance tuning.
  - ACSYS has also an expertise in FreeRTOS porting.

This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Prerequisites and related courses

- This course provides an overview of the ARM Cortex-M0 core. Our course reference RM0 - Cortex-M0 / Cortex-M0+ implementation course details the operation of this core.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

ARCHITECTURE OF STM32F0 MCUs

- ARM core based architecture
- Description of STM32F050X and STM32F051X SoC architecture
- Clarifying the internal data and instruction paths: AHB-lite interconnect, peripheral buses, AHB-to-APB bridges
- Private Peripheral Bus (PPB)
- Integrated memories
- SoC mapping

THE ARM CORTEX-M0 CORE

- V6-M core family
- Core architecture
- Programming
- Exception behavior, exception return
- Basic interrupt operation, micro-coded interrupt mechanism

BECOMING FAMILIAR WITH THE IDE

- Acsys covers 3 IDEs: Keil, IAR and GCC / Lauterbach
- Thus the customer has just to indicate which one he has chosen
- Getting started with the IDE
- Parameterizing the compiler / linker
- Creating a project from scratch
- C start program

PROGRAMMING AND DEBUGGING

- Debug interface
- Programming

RESET, POWER AND CLOCKING

- Power control
- Reset
- Clocking
- Low power modes

INTERNAL INTERCONNECT

- Bus matrix
- DMA

HARDWARE IMPLEMENTATION

- Power pins
- Pinout
- GPIO module
- System configuration controller
- External Interrupts

INTEGRATED MEMORIES

- Embedded flash memory
- Internal SRAM

TIMERS

- Advanced-control timers TIM1
- General-purpose timers (TIM2 and TIM3)
- General-purpose timers (TIM14-17)
- Basic timers (TIM6)
- Real Time Clock
- Independent Watchdog
- Window Watchdog

ANALOG MODULES

- 12-bit Analog-to-Digital Converter and Programmable Gain Amplifier
- 12-bit Digital-to-Analog Converter
- Comparator

INTEGRITY

- CRC calculation unit

CONNECTIVITY AND COMMUNICATION

- SPI
- SPI in I2S mode
- USART
- I2C

OTHER INTERFACES

- Touch sensing interface
- HDMI-CEC