STR15 - STM32G4

This course describe the STM32G4 architecture and practical examples

Objectives

- Understand the Cortex-M4F core, DSP and FPU basics.
- Configure RCC and clocks; validate timing and prescalers.
- Use GPIO/EXTI, timers, DMA/DMAMUX, and LPTIM/RTC.
- Acquire high-rate analog data with ADC + DMA, oversampling, OPAMP/COMP, DAC.
- Apply HRTIM for power/motor control; trigger ADC from PWM.
- Accelerate math with CORDIC and FMAC; compare vs software.
- Implement robust comms (USART, SPI, I²C, optional FDCAN).
- Manage Flash/OB, watchdogs, reset causes; build a production checklist.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- Practical activities
  - Practical activities represent from 40% to 50% of course duration.
  - Code examples, exercises and solutions
  - For remote trainings:
    - One Online Linux PC per trainee for the practical activities.
    - The trainer has access to trainees' Online PCs for technical and pedagogical assistance.
    - QEMU Emulated board or physical board connected to the online PC (depending on the course).
    - Some Labs may be completed between sessions and are checked by the trainer on the next session.
  - For face-to-face trainings:
    - One PC (Linux ou Windows) for the practical activities with, if appropriate, a target board.
    - One PC for two trainees when there are more than 6 trainees.
  - For onsite trainings:
    - An installation and test manual is provided to allow preinstallation of the needed software.
    - The trainer come with target boards if needed during the practical activities (and bring them back at the end of the course).
- Downloadable preconfigured virtual machine for post-course practical activities
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

Day 1

Cortex-M4F overview (core)

- Core architecture
- Programmer's model
- Exceptions, NVIC priorities.
- DSP instructions (SIMD/MACC).
- FPU single-precision.
- WFI/WFE basics.

Exercise: Exception Management
Exercise: SIMD demo

SoC & memory map

- Bus matrix AHB/APB.
- Flash/SRAM regions.
- Peripheral address map.
- UID / Flash size regs.
- Option bytes (overview).

Exercise: Map & IDs

RCC — reset & clocks

- HSI/HSE/PLL sources.
- PLLs
- SYSCLK mux, AHB/APB prescalers.
- Kernel clocks (CCIPR).
- MCO output, CSS.

Exercise: Clock profiles

GPIO / EXTI / SYSCFG

- Modes: PP/OD, pulls.
- Speed/drive strength.
- AF mapping rules.
- EXTI lines and priorities.
- Safe I/O at reset.

Exercise: GPIO / EXTI

General timers (+ LPTIM)

- PWM edge/center.
- Input capture, one-pulse.
- Encoder interface.
- Master/slave triggers.
- LPTIM for tickless.

Exercise: PWM + capture

Day 2

DMA / DMAMUX

- Stream/channel mapping.
- Circular vs normal.
- HT/TC/TE IRQs.
- Throughput vs latency.
- Restart on errors.

Exercise: UART RX ring

ADC (fast) & triggers

- Resolution & sampling time.
- Oversampling & alignment.
- Timer/HRTIM triggers.
- DMA continuous/circular.
- Analog watchdog.

Exercise: ADC + DMA stream

OPAMP / COMP / DAC

- OPAMP PGA modes.
- COMP thresholds/hysteresis.
- Routing to timers/EXTI.
- DAC 12-bit with S&H.

Exercise: Signal chain

CORDIC & FMAC (accelerators)

- CORDIC trig/vectoring.
- FMAC FIR/IIR blocks.
- Stream I/O with DMA.
- Latency vs CPU DSP.

Exercise: CORDIC vs SW

Third Day

HRTIM - high-resolution timer

- Timer units & outputs.
- Dead-time & break inputs.
- Complementary PWM pairs.
- Sync & ADC trigger points.
- Fault handling basics.

Exercise: HRTIM PWM pair

Control-loop building blocks

- PWM → ADC sampling.
- Scaling & fixed-point tips.
- Saturation & anti-windup.
- Simple PI step test.
- Update rate budgeting.

Exercise: PI step demo

USART / SPI / I²C

- UART 8/9-bit, parity.
- RX ring + idle detect.
- SPI CPOL/CPHA, NSS.
- I²C Fm+ and timeouts.
- Bus-clear recovery.

Exercise: Comms trio

(Optional) FDCAN (device-dep.)

- Classic vs FD basics.
- Nominal/data bitrates.
- Filters & message RAM.
- Loopback/silent modes.
- Transceiver notes.

Exercise: FD loopback

Day 4

Low-power & timekeeping

- Sleep/Stop/Standby.
- Wake sources (EXTI/RTC).
- LSE vs LSI trade-offs.
- LPTIM tickless scheme.
- GPIO leakage states.

Exercise: Stop + wake

Flash, OB & robustness

- Page erase/program.
- EEPROM emulation.
- OB: RDP/WRP/BOR.
- Reset cause logging.
- Watchdogs IWDG/WWDG.

Production checklist

- Clocking proven (MCO).
- I/O safe at boot/sleep.
- ADC chain documented.
- Comms error policy.
- Version/UID/CRC tags.

Exercise: Self-audit

Bonus (time-permitting)

- CMSIS-DSP quick tips.
- Simple FFT sanity.
- FMAC FIR tuning.
- HRTIM event logging.
- ADC calibration pass.

Exercise: Quick pick: choose one mini-demo and record outcome.