

STR10 - STM32F7

This course describe the STM32F7 architecture and practical examples

Objectives

- Grasp the Cortex-M7 core, pipeline, I/D-caches, FPU, SIMD, and MPU.
- Configure clocks (HSI/HSE/PLL) and prescalers.
- Use timers (PWM, capture, encoder) and time bases confidently.
- Build fast, safe DMA paths and handle cache coherency; intro DMA2D.
- Acquire analog data with ADC + DMA; basics of DAC.
- Implement USART, SPI/I²S/SAI, I²C with robust error handling.
- Bring up storage/memory: SDMMC + FatFS, QSPI XIP, FMC SDRAM.
- Enable connectivity: Ethernet (LwIP ping) and USB OTG FS/HS (CDC).
- Apply low-power modes; measure wake latency.
- Set up boot & Option Bytes, watchdogs, and reset-cause logging for production.

Course Environment

- Theoretical course
 - PDF course material (in English) supplemented by a printed version for face-to-face courses.
 - Online courses are dispensed using the Teams video-conferencing system.
 - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- Practical activities
 - Practical activities represent from 40% to 50% of course duration.
 - Code examples, exercises and solutions
 - For remote trainings:
 - ▶ One Online Linux PC per trainee for the practical activities.
 - ▶ The trainer has access to trainees' Online PCs for technical and pedagogical assistance.
 - ▶ QEMU Emulated board or physical board connected to the online PC (depending on the course).
 - ▶ Some Labs may be completed between sessions and are checked by the trainer on the next session.
 - For face-to-face trainings:
 - ▶ One PC (Linux ou Windows) for the practical activities with, if appropriate, a target board.
 - ▶ One PC for two trainees when there are more than 6 trainees.
 - For onsite trainings:
 - ▶ An installation and test manual is provided to allow preinstallation of the needed software.
 - ▶ The trainer come with target boards if needed during the practical activities (and bring them back at the end of the course).
- Downloadable preconfigured virtual machine for post-course practical activities
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the trainee in his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed in two different ways, depending on the course:

- For courses lending themselves to practical exercises, the results of the exercises are checked by the trainer while, if necessary, helping trainees to carry them out by providing additional details.
- Quizzes are offered at the end of sections that do not include practical exercises to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
 - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites, in agreement with their company manager if applicable.

Plan

Day 1

Cortex-M7 overview (core)

- Programmer's model (R0–R15, xPSR)
- MSP/PSP, exception entry/return
- Pipeline & branch prediction
- I-Cache / D-Cache basics
- ITCM / DTCM usage
- FPU
- SIMD
- MPU regions (intro)

Exercise: Core & cache sanity

SoC & memory map

- AXI matrix, AHB/APB bridges
- Flash, SRAM1/2/3 layout
- ITCM/DTCM address zones
- Peripheral regions (APB1/APB2)
- QSPI mapped memory (XIP)
- UID / Flash size registers

RCC & power & boot

- HSI/HSE/PLL sources
- PLL M/N/P/Q settings
- AHB/APB1/APB2 prescalers
- OverDrive (216 MHz) (variants)
- Boot pins, Option Bytes
- Clock security (CSS)

Exercise: Clock profiles

GPIO / EXTI / SYSCFG

- Modes: PP/OD, pulls
- Speed/drive strength
- AF mapping rules
- EXTI lines & priorities
- Debounce choices
- Safe I/O at reset

Exercise: GPIO / EXTI

Timers (adv/gen/basic) + LPTIM

- PWM edge/center
- One-pulse mode

- Input capture
- Encoder interface
- Master/Slave triggers
- LPTIM (if present)
- Break/dead-time (adv)

Exercise: PWM + capture

DMA / DMA2 & DMA2D

- DMA1/DMA2 streams/channels
- FIFO & burst modes
- Mem2mem / P2M / M2P
- Circular/HT/TC/TE IRQs
- Coherency with D-Cache
- DMA2D blit (variants)

Exercise: UART RX DMA ring

Day 2

ADC & DAC

- ADC1..3 (12-bit)
- Regular vs injected
- Sampling time, ranks
- Timer-triggered ADC
- DMA coupling
- DAC dual channel

Exercise: ADC + DMA stream

USART / UART

- 8/9-bit, parity/stop
- Oversampling 16/8
- Blocking / IRQ / DMA
- RX ring with idle detect
- Error handling (FE/ORE)
- Wake from Stop (if used)

Exercise: Robust UART

SPI / I²S / SAI

- SPI mode CPOL/CPHA
- Data sizes, NSS
- Full-duplex DMA
- I²S basic audio path
- SAI blocks (TX/RX)

Exercise: SPI loopback DMA

I²C (and SMBus)

- Sm/Fm/Fm+ speeds
- Addr 7/10-bit
- Filters (analog/digital)
- Timeouts & bus-clear
- Clock stretching
- Error recovery

Storage & external memory

- SDMMC 1/2
- FatFS basics
- QSPI XIP mapping
- FMC SDRAM/NOR/NAND
- Cache maintenance (SCB)
- Buffer alignment rules

Exercise: SD card + FatFS

Ethernet MAC (optional)

- MII/RMII PHY link
- Descriptors & rings
- DMA settings
- LwIP minimal config
- Link/ARP/ping tests

Exercise: Eth bring-up

USB OTG FS/HS

- Device/Host roles
- FS internal / HS via ULPI
- EP/FIFO sizing
- CDC/MSC quick paths
- Low-power suspend/resume

Day 3

Caches, TCM & MPU (deep-dive)

- I-Cache enable/invalidate
- D-Cache clean/invalidate
- Cache pitfalls with DMA
- ITCM code placement
- DTCM data placement
- MPU regions & attrs

Exercise: TCM vs AXI bench

Graphics & Camera (optional)

- LTDC layers/timings
- Framebuffer in SDRAM
- DMA2D color fill/blit
- DCMI capture basics
- Simple UI primitives

Exercise: Color-bar FB

Low-power & PWR

- Sleep/Stop/Standby
- OverDrive vs Stop trade-off
- Wake sources (EXTI/RTC)
- Clock gating checklist
- Retention notes

Exercise: Stop + wake

Crypto & integrity

- CRC unit
- RNG TRNG

- HASH (SHA-1/256)
- CRYPT (AES/TDES)
- Key storage basics

Exercise: AES or CRC check

Boot, Option Bytes & update

- Boot ROM interfaces
- OB: RDP/WRP/BOR
- Dual-bank (variants)
- QSPI/SD boot ideas
- Watchdogs IWDG/WWDG
- Reset causes log

Exercise: IWDG + reset log

Production checklist (wrap-up)

- Clocking & wait-states
- Cache/MPU policy
- External memory proof
- Comms robustness list
- UID/serial/versioning
- Error counters & logs

Exercise: Self-audit sheet

Renseignements pratiques

Inquiry : 3 days