FCQ7 - T4240 QorIQ implementation

This course covers NXP QorIQs T4240 & T4160

Objectives

- This course has 6 main objectives:
  - Describing the hardware implementation, particularly the boot sequence and the DDR3 controller
  - Understanding the features of the internal interconnect and related units and mechanisms such as PAMU, CPC and stashing
  - Explaining the standard bus interface controllers, PCIe, SRIO, USB, SATA and MMC-SD
  - Describing the units which are interconnected to other modules, such as clocking, interrupt controller and DMA controller, because the boot program generally has to modify the setting of these units
  - Clarifying the operation of the Datapath Acceleration Architecture that assists the processor core in taking in charge buffer allocation, queue management, frame management and particularly incoming frame classification, pattern searching, and encryption
  - Describing the various debug units and their utilization to fix errors in a multicore / multimaster SoC.
- Products and services offered by AC6:
  - AC6 is able to assist the customer by providing consultancies
  - Typical expertises are done during board bringup, hardware schematics review, software debugging, performance tuning.
  - Note that AC6 has delivered several consultancies on NXP Netcomm SoCs to companies developing avionic equipments.

A more detailed course description is available on request at training@ac6-training.com
This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Pre-requisites

- Experience of a 32-bit processor or DSP is mandatory.
- Note that the e6500 Power core is covered in a separate course reference FCC4 - e6500 implementationcourse.

Related courses

- Ethernet and switching, reference N1 - Ethernet and switchingcourse
- IEEE1588, reference N2 - IEEE1588 - Precise Time Protocolcourse
- 10 Gigabit Ethernet, reference N3 - Ethernet 10 Gigabitcourse
- PCI express gen3, reference IC4 - PCI Express 3.0course
- RapidIO 2.1, reference IC5 - RapidIO 3.0course
- USB Full Speed High Speed and USB On-The-Go, reference IP2 - USB 2.0course
- SD / MMC, reference IS2 - eMMC 5.0course
- Serial-ATA, reference IS3 - Serial ATA IIIcourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

T4240 ARCHITECTURE

- Internal architecture
- Coherency subdomains
- Memory map, local access windows
- Highlighting data paths inside the T4240
- e6500 core integration

SOC PLATFORM

POWER, RESET AND CLOCKING

- DC and AC electrical characteristics
- Reset causes
- Reset configuration words source
- Pre-boot loader
- PCIe , SRIO Host / Agent configuration
- Clocking, system clock domains
- SerDes high speed lanes configuration

SECURE BOOT

- Objectives of trust architecture
- Internal boot ROM, secure boot sequence
- Code signing
- External tamper detection
- Run time integrity checker
- Secure debug controller

CORENET PLATFORM CACHE

- Cache operation, write-through or write-back operation
- Entry locking
- Operation as memory-mapped SRAM
- Partitioning between coherency domains
- Stashing, address-based or CoreNet signalled

PERIPHERAL ACCESS MANAGEMENT UNIT (PAMU)

- Controlling master access permissions through Logical I/O Device Number
- Address translation
- Operation mode translation
- Steps in processing of DSA operations by PAMU
- PAMU gate closed state

MULTIPROCESSOR PERIPHERAL INTERRUPT CONTROLLER

- Interrupt nesting

- Description of the 4 timers / counters
- Message interrupts
- e6500-to-e6500 interrupt capability
- Interrupt assignment

LOW SPEED PERIPHERALS

- Description of the NS16450/16550 compliant Uarts
- I2C controller
- eSPI controller

ENHANCED SDHC

- Interface to SD and MMC cards
- Transfer protocol, single block, multiple block read and write
- Internal and external DMA capabilities

USB CONTROLLERS

- Host or device support
- High-speed operation
- EHCI support, scheduling the various transactions into frames
- Integrated PHY

HARDWARE IMPLEMENTATION

THE DDR3 / 3L MEMORY CONTROLLER

- Jedec specification basics
- DDR3 fly-by architecture, write leveling
- Reset sequence, dynamic ODT, ZQ calibration
- Bank activation, read, write and precharge timing diagrams, page mode
- Initial configuration following Power-on-Reset
- Timing parameters programming
- Initialization routine
- Tuning the performance of the DDR3 controller
- Testing the memory using patterns

INTEGRATED FLASH CONTROLLER

- Functional muxing of pins between NAND, NOR, and GPCM
- Data Buffer Control
- Normal GPCM FSM
- NOR flash FSM
- NAND flash FSM
- Boot from NAND

INTEGRATED DMA CONTROLLERS

- Priority between the 4 channels
- Support for cascading descriptor chains
- Scatter / gathering

PCI EXPRESS INTERFACE

- Acting as a bridge when Root Complex
- Transaction ordering rules

- Programming inbound and outbound ATMUs
- Benefits of MSIs
- Configuration, initialization
- SR-IOV implementation, Alternative Routing ID

SERIAL RAPIDIO INTERFACE

- RapidIO port
- Accept-all mode of operation
- RapidIO doorbell and port-write unit
- Accessing configuration registers via RapidIO packets
- Programming inbound and outbound ATMUs

INTERLACKEN INTERFACE

- Chip-to-chip connection to FPGA, ASIC or TCAM
- 64B/67B data encoding and scrambling
- Using software portals to interact between software and hardware
- Guaranting lane alignment, synchronizing of the scrambler, clock compensation through metaframes
- Built in statistics counters and error counters

SATA CONTROLLERS

- SATA basics
- Support for SATA II extensions
- Electrical specification
- Bringing the SATA controller online/offline
- Native command queuing, command descriptor

DATAPATH PROCESSING SUBSYSTEM

DPAA OVERVIEW

- Definitions: buffer, buffer pool, frame, frame queue, work queue, channel
- Frame formats
- DPAA Configuration and Initialization

QUEUE MANAGER

- Objectives if this accelerator
- Frame description
- Frame queue descriptor, frame queue descriptor cache
- Frame queue state machine
- Work queues and channels
- Enqueue and dequeue portals
- Sequences to understand how frames a enqueued / dequeued
- Class and intra-class scheduling rules
- Stash transaction flow control and scheduling
- Congestion avoidance
- Order definition point implementation
- Traffic shaping through CEETM

BUFFER MANAGER

- Objectives if this accelerator
- Central resource pool management function
- External linked list LIFO

- Direct connect portals
- Buffer Pool State Change Notifications

FRAME MANAGER

- Objectives if this accelerator, parsing, classifying and distributing in-line/off-line packet
- Rx BMI features
- Tx BMI features
- Offline parsing, host command features
- Frame processing manager
- FMan controller
- Host commands
- Parser
- Key generator
- Policer
- New features:
  - IP fragmentation / re-assembly
  - Header manipulation
  - Autonomous 802.1qaz
  - Data center bridging
  - Ingress multicast

MULTI-RATE ETHERNET MAC (mEMAC)

- Physical interfaces
- MAC address recognition
- Accessing PHY registers, clause 45
- Priority Flow Control
- RMON statistic counters, carry registers

RAPIDIO MESSAGE MANAGER

- 2 inbox/outbox mailboxes (queues) for data and one doorbell message structure
- Multicasting
- Outbound segmentation units

SECURITY ENGINE

- Introduction to DES, 3DES and AES algorithms
- Job management using QMan interface
- Job descriptor parsing
- Sharing descriptors
- Selecting the authentication / cryptographic algorithm
- Run Time Integrity Checking
- Public Key Hardware Accelerator (PKHA)
- SNOW 3G Accelerator
- Data Encryption Standard Accelerator (DES)
- Cyclic Redundancy Check Accelerator (CRCA)
- Message Digest Hardware Accelerator (MDHA)
- Elliptic Curve Cryptographic Functions

PATTERN MATCHER

- Objective of this unit, identifying signatures in incoming gigabit streams
- Connection to QMan and BMan
- Support for wildcarding with no pattern explosion
- Updating the pattern database
- Definition of a regular expression

- Pattern Matcher Frame Agent
- Pattern description block caching
- Key Element Scanner, trigger stage, confidence stage
- Data Examination Engine
- Stateful Rule Engine, Stateful Rule Physical Structure, SRE instruction set

GLOBAL FUNCTIONS, DEVELOPMENT AND DEBUG

DEBUG FEATURES

- NEXUS Aurora link
- Event processing unit
- Chaining, triggering
- Watchpoint facility
- Trace buffer
- Cross-Functional Debug Components
- CoreNet debug
- OCeaN debug