This course covers NXP QorIQs P1010 & P1014

Objectives

- The course clarifies the architecture of the P1010 and P1014, particularly the operation of the coherency module that interconnects the e500 to memory and high-speed interfaces.
- Cache coherency protocol is introduced in increasing depth.
- The e500 core is viewed in detail, especially the SPE unit that enable vector processing.
- The boot sequence and the clocking are explained.
- The course focuses on the hardware implementation of the P101X.
- A long introduction to DDR SDRAM operation is done before studying the DDR3/3L SDRAM controller.
- An in-depth description of the PCI-Express port is done.
- The course explains how to implement QoS on GigaEthernet controllers.

- ACSYS has developed an optimized SPE based FFT coded in assembler language.
- Performance for 1024 complex floating point single precision samples is:
  - - 91_386 core clock cycles without reverse ordering, 94_124 with reverse ordering
- Performance for 4096 complex floating point single precision samples is:
  - - 470_778 core clock cycles without reverse ordering, 511_227 with reverse ordering
- For any information contact formation@ac6-formation.com

A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites and related courses

- Experience of a 32-bit processor or DSP is mandatory.
- The following courses could be of interest:
  - Ethernet and switching, reference N1 - Ethernet and switchingcourse
  - IEEE1588, reference N2 - IEEE1588 - Precise Time Protocolcourse
  - PCI express gen2, reference IC4 - PCI Express 3.0course
  - USB Full Speed High Speed and USB On-The-Go, reference IP2 - USB 2.0course
  - SD / MMC, reference IS2 - eMMC 5.0course
  - Serial-ATA, reference IS3 - Serial ATA IIIcourse
  - CAN bus, reference IA1 - CAN buscourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION TO P1010

SOC ARCHITECTURE

- Address map, ATMU, OCEAN configuration
- Local vs external address spaces, inbound and outbound address decoding
- Access control unit

THE e500 CORE

THE INSTRUCTION PIPELINE

- Dual-issue superscalar control, out-of-order execution
- Execution units
- Dynamic branch prediction
- Execution timing

DATA AND INSTRUCTION PATHS

- Load store unit, data buffering between LSU and CCB
- Store miss merging and store gathering
- Memory access ordering
- Lock acquisition and import barriers

THE MEMORY MANAGEMENT UNIT

- Thread vs process
- The first level MMU and the second level MMU, consistency between L1 and L2 TLBs
- TLB software reload, page attributes WIMGE
- Process protection, variable number of PID registers and sharing
- 36-bit real addressing

CACHES

- The L1 caches
- Level 2 cache, partition into L2 cache plus SRAM
- Snooping mechanism
- Stashing mechanism
- L2 cache locking
- ECC protection

PROGRAMMING

- Differences between the new Book E architecture and the classic PowerPC architecture
- Floating Point units, Double-Precision FP
- Signal Processing APU (SPU): implementation of the SIMD capability without using a separate unit
- PowerPC EABI: sections, C-to-assembly interface

EXCEPTIONS

- Critical versus non critical
- Handler table
- Syndrome registers
- Core timers

DEBUGGING

- Performance monitoring
- JTAG emulation
- Watchpoint logic

INFRASTRUCTURE

RESET, CLOCKING AND INITIALIZATION

- Voltage configuration selection
- Power-on reset sequence, using the I2C interface to access serial ROM
- Power-on reset configuration
- Power management
- Secure boot and trust architecture

e500 COHERENCY MODULE

- I/O arbiter
- CCB arbiter
- Global data multiplexor

DDR3/DDR3L SDRAM MEMORY CONTROLLER

- On-Die termination
- Calibration mechanism
- Mode registers initialization, bank selection and precharge
- Command truth table
- Bank activation, read, write and precharge timing diagrams, page mode
- Introduction to the DDR-SDRAM controller
- Initial configuration following Power-on-Reset
- Timing parameters programming

INTEGRATED FLASH CONTROLLER

- Functional muxing of pins between NAND, NOR, and GPCM
- Data Buffer Control
- Normal GPCM FSM
- NOR flash FSM
- Generic ASIC FSM
- NAND flash FSM

PCI EXPRESS INTERFACE

- 1-lane PCI Express interface
- Modes of operation, Root Complex / Endpoint
- Transaction ordering rules
- Programming inbound and outbound ATMUs
- Configuration, initialization

SATA CONTROLLER

- Electrical specification
- Native command queuing, command descriptor
- Interrupt coalescing
- Port multiplier operation
- Initialization steps

PROGRAMMABLE INTERRUPT CONTROLLER

- Interrupt sources
- Integrated timers
- Per-CPU register usage
- Nesting implementation

INTEGRATED DMA CONTROLLER

- Priority between the 4 channels
- Support for cascading descriptor chains
- Scatter / gathering
- Selectable hardware enforced coherency

PERFORMANCE MONITOR AND DEBUG FEATURES

- Event counting
- Threshold events
- Chaining, triggering
- Watchpoint facility
- Trace buffer

INPUTS/OUTPUTS

THE ETHERNET CONTROLLERS

- Address recognition, pattern matching
- Buffer descriptors management
- Physical interfaces: RGMII, SGMII
- Buffer descriptor management
- Layer 2 acceleration
- 256-entry hash table
- Direct queuing of four flows
- Management of VLAN
- Quality of service
- Filer programming
- IEEE1588 compliant time-stamping

TDM INTERFACE

- Hardware interface
- Program options for frame sync and clock generation
- Network mode of operation with up to 128 time-slots
- DMA configuration
- TDM power-down feature

- Configuring the TDM for I2S Operation

ENHANCED SECURE DEVICE HOST CONTROLLER

- Storing and executing commands targeting the external card
- Multi-block transfers
- Moving data by using the dedicated DMA controller
- Dividing large data transfers
- Card insertion and removal detection

USB CONTROLLER

- Dual-role (DR) operation
- EHCI implementation
- ULPI interfaces to the transceiver
- Dedicated DMA channels
- Endpoints configuration

SECURITY ENGINE

- Introduction to DES and 3DES algorithms
- Data packet descriptors
- Crypto channels
- Link tables
- XOR acceleration

FLEXCAN MODULES

- Message buffers, mask registers
- Time Stamp based on 16-bit free-running timer
- Short latency time due to an arbitration scheme for high-priority messages

LOW SPEED PERIPHERALS

- Description of the NS16552 compliant DUART
- I2C controllers
- Enhanced SPI

Renseignements pratiques

Inquiry : 5 days