ac6

FD2 - DSP563XX implementation

This course covers the 563XX 24-bit DSP NXP family

Objectives

- The course explains how to design a 56L307 based board
- Optimized coding examples are described
- A generic interrupt handler is introduced
- DMA channels are viewed in detail
- The course focuses on the serial ports SCI and ESSI
- Practical exercices are executed on a 56L307 board

A lot of programming examples have been developed by ACSYS to explain how to write optimized code.
• They have been developed with CodeWarrior compiler and are executed under CodeWarrior debugger.
A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites

- Basic knowledge of signal processing.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION TO DIGITAL SIGNAL PROCESSING

- Arithmetic processing of real-time signals

- Modified dual Harvard architecture : the X-memory and the Y-memory
- MAC operation
- DSP 563XX family introduction

563XX ARCHITECTURE

- Core buses
- Processing states
- Reset
- 56L307 mapping

THE DSP CORE

- The Data ALU
- The Address Generation Unit
- The Program Control Unit
- The instruction set
- C-to-assembly interface
- The PLL
- The 563XX instruction cache
- Exception management
- The debugging support
- JTAG use to access the OnCE

HARDWARE IMPLEMENTATION

- External memory addressing
- Arbitration protocol
- SRAM interface
- DRAM basics
- DRAM interface

THE DMA CONTROLLER

- Overlap between DMA channel and core
- Channel priority
- Triggering modes
- Circular buffer management

THE HOST INTERFACE

- Host interface description
- Transfer modes
- Handshaking protocols
- DMA access to HTX and HRX data registers
- Boot up using the HIO8 host port
- Programming model : host-side and DSP-side register banks

THE TRIPLE TIMER MODULE

- Timer related pins
- Triple timer modes
- Event capture
- Signal width / period measuring
- PWM
- Watchdog modes

THE ENHANCED SYNCHRONOUS SERIAL INTERFACE

- ESSI signals
- Network mode

- On-Demand mode
- ESSI exceptions
- Transmit and receive sequences

THE SERIAL COMMUNICATION INTERFACE

- SCI block diagram
- Asynchronous vs synchronous operation modes
- Baud rate selection
- Bootstrap loading from the SCI
- Asynchronous transmit and receive sequences

THE ENHANCED FILTER COPROCESSOR

- PMB interface, FMAC unit, FDM bank, FCM bank
- FIR filter options
- IIR filter options
- Multichannel mode
- Input scaling

Renseignements pratiques

Inquiry : 3 days