FK2 - Kinetis KL26z MCU Implementation

This course covers the NXP Kinetis KL26z ultra low power MCU

Objectifs

- This course has 4 main objectives:
  - Describing the hardware implementation
  - Describing the ARM Cortex-M0+ core architecture
  - Describing KL26Z128VLH4 microcontroller architecture
  - Becoming familiar with the IDE (KDS) and low level programming
- Products and services offered by ACSYS:
  - ACSYS is able to assist the customer by providing consultancies.
  - Typical expertizes are done during board bring up, hardware schematics review, software debugging, performance tuning.
  - ACSYS has also an expertise in FreeRTOS or MQX porting and uIP /LWIP stack or Interniche stack integration.

A more detailed course description is available on request at formation@ac6-formation.com
This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

First Day

Architecture of Kinetis MCUs

- ARM core based architecture
- Description of KL26z SoC architecture

The ARM Cortex-M0+ Core

- V6-M core family
- Core architecture
- Thumb instruction set
- Exception behavior
- Basic interrupt operation, micro-coded interrupt mechanism , NVIC

Programming and Debugging with KDS and Open SDA

- Debug interface (Open SDA)
- Programming

Becoming Familiar with the IDE

- Getting started with the Kinetis Development Studio (KDS) IDE
- Parameterizing the compiler / linker
- Creating a project from scratch
- Cstart code

Second Day

Reset, Power and Clocking

- Reset
- Clocking
- Operation modes

KL26Z Low Power Modes

- Power and Clock gating
- LLS (Low Leakage Stop) mode
- VLLS (Very Low Leakage Stop modes)
- Low Power Timer
- Low Leakage Wakeup Unit
- Watchdog timer (WDOG)

Internal Interconnect

- Crossbar switch
- Direct Memory Access
  - DMA
  - DMA Multiplexer

Third Day

Hardware Implementation

- Power pins
- Pinout
- GPIO module

Integrated Memories

- Internal Flash
- Internal SRAM

Timers

- Timer/PWM module (TPM)
- Low power timer (LPTMR)
- Periodic Interrupt Timer
- Real Time Clock

Fourth Day

Analog Modules

- Analog-to-digital converters (ADC)
- Analog comparators
- 6-bit digital-to-analog converters (DAC)
- 12-bit digital-to-analog converters (DAC)
- Voltage Reference VREF (opt.)

USB

- USB Full-Speed OTG Controller
- USB Voltage Regulator (opt.)

Connectivity and Communication

- SPI
  - Overview and Functional description
  - Run mode
  - Low Power
- Wait mode
- Stop mode
- UART
  - Functional description
  - Register Definition
- I2C
  - Overview
  - I2C description
  - Memory map – Register definition

Human-machine interfaces

- General purpose input/output (GPIO)
  - Functional description
  - Register Definition