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This course describes the i.MX8m Dual and Quad core SoC

OBJECTIVES

- The course details the hardware implementation of the i.MX8m SoC
- The course focuses on the boot sequence, the clocking and the power management strategies
- The course explains all parameters that affect the performance of the system in order to easily perform the final tuning
- The multiple complex units involved in multimedia management are covered in depth
- An overview of the Cortex-A53 core helps to understand issues caused by MMU, cache and snooping
- Interrupt management through ARM GIC is explained through a lab
- The course also covers the hardware implementation, particularly the DDR3 and NAND flash controllers

This course is only provided on-demand; A more detailed course description is available on request at formation@ac6-formation.com
This document is necessary to tailor the course to the specific customer needs and to define the exact schedule.
Due to the large number of peripherals included in this chip, some will have to be described very briefly to fit in teh 5-days timeframe; these will be chosen according to the needs of the attendance.

Prerequisites and related courses

- This course provides only an overview of the Cortex-A53
- Our course reference RA7 - CORTEX-A53 implementation, ARM Architecture V8course details the operation of this complex ARM CPU.
- Our course reference RC2 - NEON-v8 programmingcourse explains how to vectorize and implement algorithms to be executed by ARMv8 NEON SIMD engine.

- The following courses could be of interest:
  - USB Full Speed High Speed and USB On-The-Go, reference IP2 - USB 2.0course
  - Ethernet and switching, reference N1 - Ethernet and switchingcourse
  - IEEE1588, reference N2 - IEEE1588 - Precise Time Protocolcourse
  - CAN bus, reference IA1 - CAN buscourse
  - Memory cards, reference IS2 - eMMC 5.0course
  - SATA, reference IS3 - Serial ATA IIIcourse
  - PCI Express, reference IC4 - PCI Express 3.0course

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

Architecture of the i.MX8m

- ARM core based architecture
- On-chip memories
  - Boot ROM
  - Internal multimedia / shared, fast access RAM (OCRAM, 256KB)
  - Secure/non-secure RAM (16 KB)
- Clarifying the internal data paths: AXI interconnect, AHB bus, peripheral buses
- Organization of a board based on i.MX8
- Summary of all peripheral features
- Memory mapping

System Control

- IOMUX module, understanding how to select the function supported by each pin
- Pad settings
- General Purpose Input interrupt request capability
- Signal description
- Hardware implementation, external clock sources

The Arm Cortex-A53 Core – Overview

- Presentation of the core, architecture and programming model
- Instruction sets
- Pipeline description
- MMU and TLBs
- Level 1 caches
- Cache coherency
- Level2 cache
- Timers and watchdogs

The Cortex-A53 Platform

- Cortex-A53 IP instantiation options
- Integrated interrupt controller (GIC), detail of interrupt mapping
- AHB to IP Bridge
- AHB-to-APBH Bridge with DMA
- AXI interconnect, arbitration, QoS and tide-marks parameters
- Timers, EPIT, GPT, WDOG

Reset and Clocking

- Power supplies
  - Power supplies requirements and restrictions
  - Power-up and power-down sequences
  - DC/DC and LDO supplies for on-chip resources, detail of analog regulators
  - Brownout detecto
  - Temperature monitor
- Clock Control Module

  - Clock inputs
  - Integrated PLLs, output frequency calculation
  - Frequency scaling procedure
  - Detail of clock generation circuits
  - Supporting DVFS techniques for low power modes
  - Flexible clock gating control scheme
- System Reset Controller
  - Global reset vs warm reset
  - System boot mode selection
  - Bootstrap mode operation
  - eFUSE configuration
  - Example: booting from eMMC
- General Power Controller
  - Power saving techniques
  - Uses SW State Retention, and Power Gating for ARM and NEON/VFP
  - Support for various levels of system power modes (WFI, WAIT, STOP, STANDBY)
  - Load tracking
  - Low power modes supply current

Debug Architecture

- Introduction to CoreSight, DAP features
- System Secure Controller SJC
- Embedded Trace Macrocell
- Cross Triggering Interfaces

System Security

- ARM TrustZone architecture
  - System JTAG controller
  - DDR Memory secure region protection by TrustZone Address Space Controller
- Cryptographic Acceleration and Assurance Module
  - 16-KB secure RAM
  - Violation/Tamper detection & reporting
- Secure Non Volatile Storage
  - Secure Real Time Clock
- Run-Time Integrity Checker
  - SHA-1 and SHA-256 message authentication
  - Segmented data gathering
  - One-time hash mode vs continuous hash mode
- Central Security Unit
  - Configuration during boot by eFuses
  - eFuses description
  - On-Chip OTP controller
  - Fuse shadow memory footprint
- Boot sequence
  - Boot modes
  - Boot security settings
  - Signature of the flash checking: SHA-256, 2048-bit RSA key
  - CSU and TrustZone initialization
  - Boot block activation
  - Clocks at boot time
  - Interrupt handling
  - Firmware configuration block
  - Image vector table and boot data
  - Device Configuration Data (DCD)
  - MMC and eMMC Boot
  - Boot from serial devices

Smart DMA Controller

- Overview, basic script routines
- Mapping DMA requests to channels
- Channel priority definition
- Scheduler, DMA request scanning, next channel decision tree
- CRC calculation unit
- SDMA initialization
- Instruction description
- PCU states
- Context switching
- Reference clocks and low power modes

Accessing External Memories

- Multi-Mode DDR Controller
  - Introduction to LPDDR2 and DDR3
  - Enhanced DDR3 SDRAM controller
  - Pinout, DDR calibration and delay-lines
  - Tracking open memory pages
  - Arbitration between the pending read and write accesses
  - Reordering mechanism to find the winner access
  - DDR controller debug
  - Integrated profiling tools
- General-Purpose Media Interface
  - 8-bit NAND-flash, support for raw MLC/SLC, 2/4/8 KB page size
  - ONFI2.2 compliant
  - BCH ECC up to 40-bit, hardware accelerator
  - APBH_DMA, DMA engine to drive the GPMI module
- QuadSPI Flash with support for XIP
- EIM unit
  - Support for multiplexed address / data bus operation x16 and x32 port size
  - Clarifying max address ranges per chip-select
  - NOR flash, SRAM/PSRAM control
  - Synchronous and asynchronous operation modes
  - Using DMA request to enable a slave connected to EIM to request a transfer

Mass-Storage Interfaces

- Ultra SDHC
  - 4 controllers
  - SD, MMC and SDIO protocols support
  - Transfer protocol, single block, multiple block read and write
  - Internal DMA capabilities

Multimedia

- A simple processing flow of Multimedia application
  - Display / sensor MIPI interfaces, integrated D-PHY
- Video Processing Unit
  - Multi-standard video codec
  - Frame buffer configuration
  - Hardware decoding / encoding formats up to 1080p 30fps
  - Embedded BIT processor
  - Encoding and decoding pipelines
  - Video Codec processing buffer requirement
- Image Processing Unit v3
  - Connectivity to displays and controllers (Parallel, LVDS, MIPI, HDMI), cameras (parallel, MIPI)
  - Video Input Ports Connectivity

  - Video acquisition, CSI interface
  - Synchronization, still image capture, video mode
  - Image Signal Processor, processing captured images
  - Processing chain description
  - Image conversions: resizing, rotation/inversion, color conversion, deinterlacing
  - Display signals muxing chain
  - LVDS display bridge
  - Display port, synchronous access vs asynchronous access
  - HDMI 1.4 interface, HDCP support
  - Video Data Order Adapter
  - Display Content Integrity Checker, verifying that a safety-critical information sent to a display is not corrupted
  - IPU debug facilities
- Graphics Processing Unit
  - Host and Memory Interface Features
  - Power management Features
  - Command Processor Features
  - OpenCL Support
  - Texture Processing
  - Fragment Processing
  - Rendering
  - Destination and Alpha Blending
  - GPU Usage

Audio Related Interfaces

- Overview of audio subsystem
- SSI interfaces
  - Connection of Codecs or DSPs
  - I2S mode
  - Frame synchronization
  - AC97 support
- Digital audio multiplexor
  - Connecting host interfaces to peripheral interfaces
  - External signal description
  - Internal network mode
- SPDIF transmitter
  - Introduction to IEC958
  - Selecting the clock
  - Transmit FIFO operation
- Enhanced Serial Audio Interface (ESAI)
- Asynchronous Sample Rate Converter
  - Concurrent sample rate conversion of up to 10 channels
  - User-programmable threshold for the input/output FIFOs
  - Word alignment supported
- PWM
  - 16-bit counter, optimized to generate sound from stored sample audio images
  - 4 x 16 data FIFO
  - Can be programmed to be active in low power and debug modes

PCIe Controller

- Gen 2 operation
- 1-lane
- Configuration as Agent or Root Complex
- Interrupt management
- Error management
- PHY setting

Communication Controllers

- HSI
- o PIO and DMA access modes
  - 16 logical channels for both transmit and receive operation
  - Per-channel programmable bandwidth
  - Configurable transmit and receive FIFO
  - Data channel buffer management, DMA engine
- Enhanced CSPI
  - SPI protocol basics
  - Master / slave operation
  - External chip-select
  - FIFO mode, DMA support
- I2C interfaces
  - I2C protocol basics
  - Master vs slave
  - Transfer sequence
- UART
  - 8-wire vs 4-wire UART controllers
  - Support for Smart Card
  - Flow control
  - Supporting 9-bit RS485 multidrop mode
- USB
  - Explaining what is OTG
  - The 4 USB ports
  - High-speed operation
  - EHCI support
  - ULPI bypass mode
  - Full speed operation
  - Endpoint configuration
- Gigabit Ethernet Controller
  - Ethernet basics
  - PHY connection, PHY management interface
  - Buffer management, based on Buffer Descriptors
  - Incoming frame filtering mechanisms, hash tables
  - Flow control in Full Duplex mode
  - VLAN support
  - TCP-IP offload
  - IEEE1588 protocol support, timestamp registers
- MediaLB
  - Interface to MOST networks
  - 3- or 6-pin operation
  - MediaLB PLL
  - Host bus interface block
  - Routing fabric block
  - Management of asynchronous and isochronous channels
  - Channel descriptor table
  - Single vs Multiple packet mode
- FlexCAN controllers
  - CAN protocol basics
  - Flexible mailboxes of zero to eight bytes data length
  - Individual Rx Mask Registers per mailbox
  - Time Stamp based on 16-bit free-running timer

Renseignements pratiques

Inquiry : 5 days