U1 - SystemVerilog

SystemVerilog for RTL Design and Functional Verification

Objectives

- Understand the role of SystemVerilog in modern digital design and verification environments
- Differentiate between simulation and synthesis, and apply appropriate coding practices
- Master SystemVerilog data types, including integral, composite, and dynamic structures
- Develop efficient RTL code using procedural blocks and proper assignment techniques
- Apply control flow, parallel processing, and casting for robust hardware modeling
- Design scalable systems using modules, interfaces, packages, and hierarchical constructs
- Understand simulation scheduling semantics and avoid race conditions in designs
- Apply object-oriented programming concepts for verification using classes and inheritance
- Create constrained-random test scenarios using randomization and constraints
- Measure and improve design quality using functional and code coverage techniques
- Use assertions to validate design behavior and detect errors early in simulation
- Develop structured test benches using interfaces and basic verification components
- Understand the fundamentals of UVM and its role in modern verification methodologies

Prerequisite

- Basic knowledge of digital design concepts (combinational and sequential logic)
- Familiarity with Verilog or VHDL (RTL coding fundamentals)
- Understanding of simulation concepts and waveform analysis
- Basic programming knowledge (C/C++ or similar is a plus)
- Familiarity with FPGA or ASIC design flow is recommended but not mandatory

Course environment

- Theoretical course
  - PDF course material (in English)
  - The trainer to answer trainees questions during the training and provide technical and pedagogical assistance
- Practical activities
  - Practical work with ModelSim QuestaSim and Vivado Simulator.
  - Practical activities represent from 40% to 50% of course duration
  - Example code, labs and solutions

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline