IP1 - FireWire

This course covers IEEE1394, IEEE1394a, IEEE1394b and DV specification

Objectives

- Differential transmission advantages are highlighted.
- The course explains the bus initialization process.
- Packet format and subaction transactions are described with the assistance of the Lecroy FireInspector
- 1394a arbitration enhancements are emphasized.
- The course describes the new 1394b beta signalling.
- After having introduced digital camera fundamentals, isochronous traffic is analysed.
- The OHCI specification and especially the management of transfer descriptors is also handled in this course.

A Lecroy FireWire analyser wasused to capture and display FireWire traffic.
• A lot of traces are included in the material.
A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites

- Experience of a digital bus is mandatory.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

1394-1995 OVERVIEW

- Bus creation and history
- 1394 bus architecture
- Technical introduction : time-slicing
- Support of asynchronous and isochronous transactions
- Protocols stack : AVC, SBP-2, 1883, HAVI, IP

LAYER MODEL

- Unified transactions
- The transaction layer
- The link layer
- The physical layer
- The management layer

- Protocol implementation, highlighting the separation between software and hardware domains

HARDWARE IMPLEMENTATION

- LVDS technology basics
- Data and strobe encoding
- Line states for arbitration, configuration and reset
- Decoding rules
- Idle bus delays to enable arbitration requests : the gaps
- Power Classes
- Suspend / Resume mechanism

SOFTWARE INTERFACE

- IEEE1212 address definition and node mapping
- Link layer Control & Status Registers
- Link layer configuration ROM organization
- PHY layer registers
- TI 12LV22 programming interface to access local PHY registers

BUS INITIALIZATION

- Reset causes
- Initialization steps
- Tree building, contention resolution
- Self-ID process, Self-ID packet format
- Software configuration : cycle master enabling, IRM identification, Bus Manager select

1394/1394a ARBITRATION

- Geographic priority
- Arbitration for asynchronous transfers
- Arbitration for synchronous transfers
- Inefficiency of gaps when data rate increases
- 1394a optimizations : accelerated and fly-by arbitrations

ASYNCHRONOUS TRANSACTIONS

- Read and Write REQ/RESP packet format
- Resource locking
- Retry goals
- Single-phase retry
- Transaction errors management

1394-BASED DIGITAL CAMERA SPECIFICATION

- Digital camera control command registers
- Camera initialize register
- Isochronous packet format for VGA non compressed format (Format_0)
- Video data payload structure

ISOCHRONOUS TRANSACTIONS

- Talker and listeners
- Channel number and bandwidth allocation
- Real time data flows requirements
- Packet format

PHY-LINK INTERFACE

- Pinout
- PHY register access
- Status information transmission from PHY to Link
- Packet transmission timing diagram
- Packet receipt timing diagram

1394b OVERVIEW

- New transmission media
- Bilingual ports
- Compatibility with 1394/1394a specifications

BETA SIGNALLING

- Optic transmission fundamentals
- Full duplex communication
- Scrambler / Descrambler operation
- Benefits of 8b/10b encoding
- Training sequence

1394b ARBITRATION

- Symbol use instead of gaps
- Bus requests pipelining, arbitration phases
- Arbitration in a hybrid tree including DS ports and Beta ports

CONNECTION MANAGEMENT

- Tones usage
- Auto-negotiation
- Standby / Restore mechanism
- Loop removing

1394b PHY-LINK INTERFACE

- Enhancement of the 1394a PHY-LINK interface to support S800
- New PIL-FOP interface to support higher data rates
- Point-to-point packet protocol between the PIL and the FOP

OPEN HOST CONTROLLER INTERFACE

- SelfID receive
- Asynchronous transmit DMA
- Asynchronous receive DMA
- Isochronous transmit DMA
- Isochronous receive DMA
- Physical requests
- Error management