[redacted]

This course describes the STM32MP15x SoC

Objectifs

- This course details the hardware implementation of the STM32MP15x SoC
- The course focuses on the boot sequence, the clocking and the power management strategies
- The course explains all parameters that affect the performance of the system in order to easily perform the final tuning
- An overview of the Cortex-A7MP core helps to understand issues caused by MMU, cache and snooping
- An overview of the Cortex-M4F with MPU is included to understand the microcontroller side of the STM32MP15 implementation
- To become more familiar with the synchronization features of the STM32MP15x implementation labs are proposed
- Note that this course has been designed from the architecture of STM32MP15x-series devices, the STM32MP157C
- The peripherals overview presented in this course can be detailed upon request (STR9 - STM32 Peripheralscourse)

Prerequisites and Related Courses

- Familiarity with C concepts and programming targeting the embedded world
- Basic knowledge of embedded processors
- The following courses could be of interest:
  - RA4 - Cortex-A7 implementationcourse
  - RM3 - Cortex-M4 / Cortex-M4F implementationcourse
  - STR9 - STM32 Peripheralscourse
  - OS3 - FreeRTOS Programmingcourse
  - D1S - Embedded Linux with Ac6 System Workbenchcourse
  - D1Y - Embedded Linux with Yoctocourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- Practical activities
  - Practical activities represent from 40% to 50% of course duration.
  - Code examples, exercises and solutions
  - For remote trainings:
    - One Online Linux PC per trainee for the practical activities.
    - The trainer has access to trainees' Online PCs for technical and pedagogical assistance.
    - QEMU Emulated board or physical board connected to the online PC (depending on the course).
    - Some Labs may be completed between sessions and are checked by the trainer on the next session.
  - For face-to-face trainings:
    - One PC (Linux ou Windows) for the practical activities with, if appropriate, a target board.
    - One PC for two trainees when there are more than 6 trainees.
  - For onsite trainings:
    - An installation and test manual is provided to allow preinstallation of the needed software.
    - The trainer come with target boards if needed during the practical activities (and bring them back at the end of the course).
- Downloadable preconfigured virtual machine for post-course practical activities
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed in two different ways, depending on the course:
  - For courses lending themselves to practical exercises, the results of the exercises are checked by the trainer while, if necessary, helping trainees to carry them out by providing additional details.
  - Quizzes are offered at the end of sections that do not include practical exercises to verifythat the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

First Day

Cortex M4 Architecture Overview

- V7-M Architecture Overview
- Core Architecture
  - Harvard Architecture, I-Code, D-Code and System Bus
  - Write Buffer
  - Registers (Two stacks pointers)
  - States
  - Different Running-modes and Privileged Levels
  - System Control Block
  - Systick Timer
  - MPU Overview
- Programming
  - Alignment and Endianness
  - CMSIS Library
- Exception/ Interrupt Mechanism Overview
  - Vector Table
  - Interrupt entry and return Overview
  - Tail-Chaining
  - Pre-emption (Nesting)
  - NVIC Integrated Interrupt Controller
  - Exception Priority Management
  - Fault escalation
- Debug Interface

Exercise: *Becoming familiar with the IDE and Clarifying the boot sequence*
Exercise: *Cortex-M4 Mode Privilege*
Exercise: *Cortex-M4 Exception Management*
Exercise: *Cortex-M4 MPU*

The ARM Cortex-A7MP Architecture Overview

- V7-A Architecture Overview
- Cortex A7 Overview
  - Cortex-A7 Architecture
  - Hardware Cache Coherency

  - Cortex-A7 Main Features
- System Features
  - Multi-processing
  - Cache Maintenance
  - Cache Coherency Hardware
  - Interrupt Distribution
  - Power saving Modes
  - Memory System Hierarchy
  - Software Storage and Upload
- Memory Management Unit
- Generic Interrupt Controller
- Multicore operation
- TrustZone
- Virtualization Extension

Second Day

STM32MP15 Architecture Overview

- ARM Core Based Architecture
- Description of STM32MP15 SoC architecture
- Clarifying the internal data and instruction paths:
  - Bus Architecture
  - NIC-400 Network Interconnect AXI-based
  - Multi-Layer AHB Interconnect
- Memory Organization
  - Embedded Memories: (ROM, SYSRAM, MCU SRAM, Retention RAM
  - External Memories: (DDR3/LPDDR2, FMC, QUADSPI, SDMMCx)
- SoC mapping
- Boot Configuration

Boot, Security and One time programmable (OTP) control (BSEC)

- Introduction
- BSE Block diagram
- Interface to OTP
- OTP security Mode
- OTP operations
  - OTP read
  - OTP programming
  - OTP permanent write lock
- Scratch registers and Transport key (TK) access
- OTP Mapping

Reset, Power and Clocking

- Power Control
  - Power control overview
  - Power supplies
  - Power supply supervision
  - Power management
  - Low-Power Modes
  - Power control interrupts
  - Power Control and TrustZone capability
- RCC Reset and Clock
  - RCC overview
  - RCC Block diagram
  - RCC Reset
  - RCC Clock

  - RCC interrupts
  - Handling dynamic Clock switching
  - PLL Programming
  - Configuring the sub-system clock
  - Clock calibrations using timers

Exercise: *Configure the system to measure the current consumption in different low-power modes (Cortex-M4)*
Exercise: *RTC wakeup timer event / interrupt (Cortex-M4)*
Exercise: *Configure the system Clock (SYSCLK) and modify the clock settings in Run Mode (Cortex-M4)*

Synchronizations mechanisms

- Hardware Semaphore (HSEM)
  - HSEM Overview
  - Lock procedures
  - Clear Procedures
  - Interrupts
- Inter-Processor Communication Controller (IPCC)
  - IPCC Overview
  - Simplex Channel and Half-Duplex channel modes
  - IPCC interrupts

Third Day

Hardware Implementation

- Power pins
- Pinout
  - Pin Muxing, alternate functions
- GPIO Module
  - Configuring a GPIO
  - Speed selection
  - Locking mechanism
  - Analog function
  - Integrated pull-up / pull-down
  - I/O pin multiplexer and mapping
  - TrustZone security
- System Configuration Controller
  - I/O compensation cell
  - Ethernet Clock source
- Interrupts
  - Nested Vectored Interrupt Controllers (NVIC)
  - Global interrupt Controller (GIC)
  - Extended Interrupt and event controller (EXTI)

Exercise: *How to configure the external interrupt lines*

Internal Interconnect

- Bus Matrix
- DMA

Exercise: *DMA FIFO mode*

Security and Integrity

- Extended TrustZone Protection Controller
  - Extended Trustzone architecture and ETZPC
  - STM32P15x Security Architecture
  - STM32P15x MCU resource isolation
- True Random number generator (RNG)
- Hash processor (HASH)

- Cryptographic Processor (CRYP)

Exercise: *CRC User Defined Polynomial*
Exercise: *How to use ASH peripheral to hash data with SHA-1 and MD5 algorithms*
Exercise: *How to use the Cryptographic Processor*

Memory Features

- DDR3/LPDDR2/LPDDR3 Controller (DDRCTRL)
  - DDRCTLR Architecture overview
  - Transaction Service Control and QoS
  - Power saving
  - Address mapper
  - DRAM timing parameters
  - SDRAM initialization sequence
  - Refresh controls
  - DDRCTRL Configuration
  - TrustZone Address Space Controller for DDR
- DDR physical Interface Control (DDRPHYC)
- DDR performance monitor (DDRPERFM)
- Master Direct Memory Access (MDMA) Controller
- Flexible Memory Controller (FMC)
- Quad-SPI interface
- Delay Block

Exercise: *Configuring the FSMC controller to access the SRAM memory*
Exercise: *QSPI Read Write IT*

Fourth Day

Asymmetric Multiprocessing Communication

- Open AMP-Overview
- Components in OpenAMP
- Connection between OpenAMP and Libmetal
- How to write a simple OpenAMP application
- CoProSync APIs

Exercise: *Creating rpmsg channel between Cortex-M4 and Cortex-A7MP (Cortex-M4 side)*

Analog modules

- Analog-to-Digital (ADC)
- Digital-to-Analog Converter (DAC)
- Digital filter for sigma delta modulators (DFSDM)
- Temperature sensor (TDS)

Exercise: *ADC Single Conversion Trigger Timer DMA*

Fifth Day

Watchdogs and Real-time clock (RTC)

- Independent Watchdogs (IWDG)
- Window Watchdog
- RTC
  - Overview
  - Functional Description
  - RTC low power-modes

Exercise: *MCU WWDG reset*
Exercise: *RTC Alarm*

Connectivity and communication

- SPI
- USART/UART
- I2C
- Serial audio interface & DPDIF receiver interface
- Management data input/output (MDIOS)
- Secure Digital input/output MultiMediaCard Interface
- FDCAN
- USB OTG
- USB HS PHY controller
- USB EHCI/USB_OHCI
- HDMI-CEC
- Ethernet

Exercise: *How to handle I2C data buffer Tx/Rx between two boards via DMA*

Debug Support

- Debug block diagram
- Debug power and clocking
- Security
- Chip Level TAP controller
- Serial wire and JTAG debug port (SWJ-DP)
- Access port
- Cortex-A7 debug
- Cortex-M4 debug

Renseignements pratiques

Inquiry : 5 days