FPQ8 - MPC834X implementation

This course covers PowerQUICC II Pro MPC834X processors, such as MPC8349A

Objectives

- The course focuses on the sequencer that interconnects e300, DDR SDRAM, PCI and external bus.
- Cache coherency protocol is introduced in increasing depth.
- The 32-bit e300 core is viewed in detail, especially the MMU and the cache.
- The boot sequence and the clocking are explained.
- The course focuses on hardware implementation of the MPC834X.
- A long introduction to DDR SDRAM operation is done before studying the DDR SDRAM controller.
- An in-depth description of the PCI controllers is performed.
- The course highlights both hardware and software implementation of gigabit / fast / Ethernet controllers.
- The USB interfaces are also detailed.
- Generation of a Linux image and Root File System by using LTIB can also be included into the training.

- This course has been delivered several times to companies developing avionics equipments.

A lot of programming examples have been developed by ACSYS to explain the boot sequence and the operation of complex peripherals, such as USB and Ethernet.

- *They have been developed with Diab Data compiler and are executed under Lauterbach debugger.*

A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites and related courses

- The knowledge of the following interconnect standards may be required:
  - PCI, see our course reference IC1 - PCI 3.0course
  - Gigabit Ethernet, see our course reference N1 - Ethernet and switchingcourse
  - USB 2.0, see our course reference IP2 - USB 2.0course

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented

- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION TO MPC834X

OVERVIEW

- General features
- Enhancements compared to MPC824X
- Block diagram
- Features of the MPC8343E, MPC8347E, MPC8349E and MPC8349EA

THE e300 CORE

THE INSTRUCTION PIPELINE

- Pipeline basics
- Branch processing unit
- Branch instructions
- Simplified branch mnemonics

DATA PATHS

- Load / store buffers
- Sync and eieio instruction

CACHES

- Cache basics
- Cache locking
- L1 caches
- Cache coherency mechanism
- The MEI state machine
- Management of cache enabled pages shared with PCI DMAs
- Reservation coherency
- Cache related instructions
- Software enforced cache coherency
- Cache flush routine

SOFTWARE IMPLEMENTATION

- PowerPC architecture specification, the 3 books UISA, VEA and OEA
- e300 registers
- Addressing modes, load / store instructions
- Integer instructions
- Rotate instructions : inserting and extracting bitfields
- IEEE754 basics, floating points numbers encoding
- The PowerPC EABI

THE MMU

- Thread vs process
- Introduction to real, block and segmentation / pagination translations

- Real mode restrictions
- Memory attributes and access rights definition
- Virtual space benefit, page protection through segmentation
- TLBs organization
- Pagination : PTE table organization, tablesearch algorithm
- Explanation of hash value and API field
- MMU implementation in real-time sensitive applications

THE EXCEPTION MECHANISM

- MSR, SPRG0-3, DAR and DSISR supervisor registers description
- Save / restore registers SRR0/SRR1, rfi instruction
- Exception management mechanism
- Requirements to allow exception nesting

THE DEBUG PORT

- JTAG emulation, restrictions
- Real time trace requirements
- Code instrumentation
- Hardware breakpoints

THE PLATFORM CONFIGURATION

POWER, RESET AND CLOCKING

- DC and AC electrical characteristics
- Power management control
- Reset causes
- Reset configuration words source, boot from I2C or boot from EEPROM
- PCI Host / Agent configuration, PCI1 and PCI2 arbiter configuration
- Clocking in PCI Host mode
- External clock inputs
- System PLL ratio
- Delay Locked Loop

ADDRESS TRANSLATION AND MAPPING

- Local memory map
- Local access windows
- Inbound and outbound windows definition

ARBITER AND BUS MONITOR

- External signal description
- PCI outbound window definition
- Transaction forwarding

SEQUENCER

- Coherent system bus overview
- Bus error detection
- Initialization sequence

GENERAL PURPOSE INPUTS / OUTPUTS

- Pin model
- Direction definition
- Interrupt inputs

THE DDR MEMORY CONTROLLER

- DDR-SDRAM operation
- Jedec specification basics, mode register initialization, bank selection and precharge
- Hardware interface
- Bank activation, read, write and precharge timing diagrams, page mode
- ECC error correction
- DDR-SDRAM controller introduction
- Initial configuration following Power-on-Reset
- Address decode
- Timing parameters programming
- Initialization routine

LOCAL BUS CONTROLLER

- Multiplexed 32-bit address and data transfers
- Burst support
- Dynamic bus sizing
- GPCM, UPMs and NFC states machines

PCI BUS INTERFACES

- Bridge features
- Data flows : Read prefetch and write posting FIFOs
- Inbound transactions handling, Outbound transactions handling in both modes
- PCI bus arbitration
- PCI hierarchy configuration

INTEGRATED DMA CONTROLLER

- Priority between the 4 channels
- Support for cascading descriptor chains
- Scatter / gathering
- Selectable hardware enforced coherency
- Concurrent execution across multiple channels with programmable bandwidth control
- Messaging unit
- Doorbells management

INTEGRATED PROGRAMMABLE INTERRUPT CONTROLLER

- Interrupt masking
- Definition of interrupt priorities
- Interrupt management, vector register
- Requirements to support nesting
- Machine check interrupts

TIMERS

- Software watchdog timer
- Real time clock module
- Periodic Interval Timer
- General Purpose Timers, cascaded modes, capture operation

INTEGRATED PERIPHERALS

SECURITY ENGINE

- Introduction to DES and 3DES algorithms

- Data packet descriptors
- Crypto channels
- Link tables

THE ETHERNET CONTROLLERS

- 802.3 specification fundamentals
- Address recognition, pattern matching
- MII interface
- Buffer descriptors management
- The three-speed Ethernet controllers (TSECs)
- Physical interfaces : GMII, MII, TBI or RGMII
- Buffer descriptor management
- Layer 2 acceleration accept or reject on address or pattern match
- 256-entry hash table for unicast and multicast

THE USB 2.0 CONTROLLERS

- Multi-port host (MPH) and dual-role (DR) module
- EHCI implementation
- UTMI / ULPI interfaces to the transceiver
- OTG support
- Dedicated DMA channels
- Endpoints configuration
- Queue Element transfer descriptor
- Management of isochronous pipes

LOW SPEED PERIPHERALS

- Description of the NS16450/16550 compliant Uarts
- FIFO mode
- Flow control signal management
- I2C protocol fundamentals
- Transmit and receive sequence
- SPI protocol basics
- Master vs slave operation

Linux Target Image Builder (LTIB)

GENERATING THE LINUX KERNEL IMAGE

- Introducing the tools required to generate the kernel image
- What is required on the host before installing LTIB
- Common package selection screen
- Common target system configuration screen
- Building a complete BSP with the default configurations
- Creating a Root Filesystems image
- e-configuring the kernel under LTIB
- Selecting user-space packages
- Setup the bootloader arguments to use the exported RFS
- Debugging Uboot and the kernel by using Trace32
- Command line options
- Adding a new package
- Other deployment methods
- Creating a new package and integrating it into LTIB
  - A lot of labs have been created to explain the usage of LTIB

Renseignements pratiques

Duration : **5 days**
Cost : **2100 € HT**