FM6 - MPC5777M implementation

This course covers the NXP Qorivva MPC5777M microcontroller

OBJECTIVES

- **This course has the following objectives:**
  - **Clarifying the architecture of the SoC, especially the split between the computanional shell and the IO complex**
  - **Providing all informations required to design a board based on MPC5777M, detailing clocking, power management and reset sequence**
  - **Describing and implementing the safety mechanisms, explaining the purpose of each unit involved in error management**
  - **Distributing interrupts to the 3 CPUs and relying on eDMA channels to transfer data between IO part and e200z7 RAMs**
- **Indicating the capabilities of debug related units, particularly the trace and watchpoint units**
  - **Detailing the communication modules, such as FlexRAY, CAN and Ethernet controllers.**
- **Products and services offered by AC6:**
  - **AC6 is able to assist the customer by providing consultancies**
  - **Typical expertises are done during board bringup, hardware schematics review, software debugging, performance tuning.**
  - **A lot of companies developing avionics systems are trusting AC6.**

They have been developed with Diab Data compiler and are executed with TRACE32 Lauterbach debugger.

A more detailed course description is available on request at formation@ac6-formation.com
This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Prerequisites and related courses

- **Experience of a 32-bit processor or DSP is mandatory.**
- **Note that the e200z7 Power core is covered in a separate course reference FCC3 - e200z7 implementationcourse.**
- **The following courses could be of interest:**
  - **FlexRay, reference IA2 - FlexRay 2.1course**
  - **CAN bus, reference IA1 - CAN buscourse**
  - **Ethernet, reference N1 - Ethernet and switchingcourse.**

Course Environment

- **Theoretical course**
  - **PDF course material (in English) supplemented by a printed version for face-to-face courses.**
  - **Online courses are dispensed using the Teams video-conferencing system.**
  - **The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.**
- **At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed**

Target Audience

- **Any embedded systems engineer or technician with the above prerequisites.**

Evaluation modalities

- **The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.**
- **Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented**
- **At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.**
  - **In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.**

Plan

ARCHITECTURE OF MPC5777M

- **Block diagram**
- **Computational shell**
- **Peripheral domain**
- **Memory hierarchy**

SAFETY MECHANISMS

- **Overview**
- **Cyclic Redundancy Check (CRC) Unit**
- **Memory Error Management Unit (MEMU)**
- **Indirect Memory Access (IMA)**
- **Fault Collection and Control Unit (FCCU)**
- **Self-Test Control Unit (STCU2)**
- **Register Protection (REG_PROT)**

CORE COMPLEX OVERVIEW

- **e200z720n3, e200z719, and e200z425n3 cores**
- **Microarchitecture summary**

EMBEDDED MEMORIES

- **Platform RAM controller**
- **Flash memory controller, flash organization**
- **Decorated Storage Memory Controller**

HARDWARE IMPLEMENTATION

- **Power supplies and reference voltages, power-up sequence**
- **Reset Generation Module**
- **GPIO multiplexing**
- **Clocking**
- **External Bus Interface**
- **Power Management Controller digital interface**
- **Wakeup Unit (WKPU)**

SYSTEM MODULES

- **Interconnect parameterizing, introduction to AHB and APB buses**
- **Sharing exclusive resources: SEMA42 unit**
- **Interrupt controllers, 64 priority levels**
- **eDMA controller**
- **Timers**

SECURITY

- **Overview**
- **Password and Device Security Module (PASS)**
- **Tamper Detection Module (TDM)**

ANALOG MODULES

- **Overview of the integrated ADCs, sample transfer to memory using DMA channels**
- **Sigma-Delta Analog-to-Digital Converter**
- **Successive Approximation Register Analog-to-Digital Converter**
- **Temperature Sensor, calculating device temperature**

COMMUNICATION MODULES

- **CAN subsystem**
- **Serial Interprocessor Interface (SIPI)**
- **LVDS Fast Asynchronous Serial Transmission (LFAST)**
- **Fast Ethernet Controller (FEC)**
- **FlexRay**
- **Deserial Serial Peripheral Interface**
- **Inter-Integrated Circuit**
- **Peripheral Sensor Interface (PSI5)**
- **SENT Receiver (SRX)**
- **LINFlexD**

CALIBRATION AND DEBUG MODULES

- **Core debug support**
- **e200z425n3 Core Debug Support**
- **e200z720n3 Core Debug Support**
- **Debug and Calibration Interface**
- **JTAG Controllers**
- **Sequence Processing Unit (SPU)**
- **Development Trigger Semaphore (DTS)**
- **Nexus Aurora Router (NAR)**
- **GTM Development Interface**
- **Emulation and Debug Device Introduction**

Renseignements pratiques

Duration : 4 days
Cost : 1950 € HT