FCQ6 - P5020 QorIQ implementation

This course covers NXP QorIQ P5010 and P5020

Objectives

- This course has 6 main objectives:
  - Describing the hardware implementation, particularly the boot sequence and the DDR3 controller
  - Understanding the features of the internal interconnect and related units and mechanisms such as PAMU, CPC and stashing
  - Describing the units which are interconnected to other modules, such as clocking, interrupt controller and DMA controller, because the boot program generally has to modify the setting of these units
  - Explaining the standard bus interface controllers, PCIe, SRIO, USB and MMC-SD
  - Clarifying the operation of the Datapath Acceleration Architecture that assists the processor core in taking in charge buffer allocation, queue management, frame management and particularly incoming frame classification, pattern searching, and encryption
  - Describing the various debug units and their utilization to fix errors in a multicore / multimaster SoC.

- Products and services offered by ACSYS:
  - ACSYS is able to assist the customer by providing consultancies
  - Typical expertises are done during board bringup, hardware schematics review, software debugging, performance tuning.
  - Note that ACSYS has delivered several consultancies on NXP Netcomm SoCs to companies developing avionic equipments.

A more detailed course description is available on request at formation@ac6-formation.com
This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Pre-requisites

- Experience of a 32-bit processor or DSP is mandatory.
- Note that the e5500 Power core is covered in a separate course reference cours FCC2 - e5500 implementation.

Related courses

- Ethernet and switching, reference cours N1 - Ethernet and switching
- IEEE1588, reference cours N2 - IEEE1588 - Precise Time Protocol
- 10 Gigabit Ethernet, reference cours N3 - Ethernet 10 Gigabit
- PCI express gen2, reference cours IC4 - PCI Express 3.0
- RapidIO 2.1, reference cours IC5 - RapidIO 3.0
- USB Full Speed High Speed and USB On-The-Go, reference cours IP2 - USB 2.0
- SD / MMC, reference cours IS2 - eMMC 5.0
- Serial-ATA, reference cours IS3 - Serial ATA III

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique

- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Modalités d'évaluation

- Les prérequis indiqués ci-dessus sont évalués avant la formation par l'encadrement technique du stagiaire dans son entreprise, ou par le stagiaire lui-même dans le cas exceptionnel d'un stagiaire individuel.
- Les progrès des stagiaires sont évalués par des quizz proposés en fin des sections pour vérifier que les stagiaires ont assimilé les points présentés
- En fin de formation, une attestation et un certificat attestant que le stagiaire a suivi le cours avec succès.
  - En cas de problème dû à un manque de prérequis de la part du stagiaire, constaté lors de la formation, une formation différente ou complémentaire lui est proposée, en général pour conforter ses prérequis, en accord avec son responsable en entreprise le cas échéant.

Plan

P5020 ARCHITECTURE

SOC ARCHITECTURE

- Block diagram
- Internal architecture
- CoreNet coherency fabric
- Coherency subdomains
- Memory map, local access windows
- Highlighting data paths inside the P5020, benefit of a dual-DDR controller system
- Application examples
- Multicore processing scenarios
- e5500 core integration

SOC PLATFORM

POWER, RESET AND CLOCKING

- Power management control
- Configuration signals sampled at reset
- Reset configuration words source
- Pre-boot loader
- Clocking, system clock domains
- Dynamically changing core clocks
- SerDes high speed lanes configuration

SECURE BOOT

- Objectives of trust architecture
- Secure boot sequence
- External tamper detection
- Run time integrity checker

CORENET PLATFORM CACHE

- Operation as memory-mapped SRAM

- Partitioning between coherency domains
- Stashing
- Soft error detection and correction

PERIPHERAL ACCESS MANAGEMENT UNIT (PAMU)

- Controlling master access permissions through Logical I/O Device Number
- Address translation
- Descriptor organization
- Operation mode translation
- Steps in processing of DSA operations by pamu
- PAMU caches

MULTIPROCESSOR PERIPHERAL INTERRUPT CONTROLLER

- Interrupt nesting
- Description of the 4 timers / counters
- Message interrupts
- e5500-to-e5500 interrupt capability

LOW SPEED PERIPHERALS

- UART
- I2C controller
- eSPI controller

ENHANCED SDHC

- Transfer protocol, single block, multiple block read and write
- Internal and external DMA capabilities
- SD protocol unit
- Card insertion and removal detection

USB CONTROLLERS

- Host or device support
- EHCI support, scheduling the various transactions into frames
- Integrated PHY
- Endpoint configuration
- Non-EHCI tuning control registers

HARDWARE IMPLEMENTATION

THE DDR3 / 3L MEMORY CONTROLLER

- DDR3 fly-by architecture, write leveling
- ZQ calibration
- Command truth table
- Hardware interface
- Initial configuration following Power-on-Reset
- Controller interleaving support
- Address decode unit
- Timing parameters programming

ENHANCED LOCAL BUS CONTROLLER

- Multiplexed or non-multiplexed address and data buses
- Connecting 8- and 16-bit devices
- Burst support

- GPCM, UPMs states machines
- NAND flash controller

INTEGRATED DMA CONTROLLERS

- Priority between the 4 channels
- Scatter / gathering
- Selectable hardware enforced coherency
- Ability to start DMA from external 3-pin interface

PCI EXPRESS INTERFACE

- Acting as a bridge when Root Complex
- Transaction ordering rules
- Programming inbound and outbound ATMUs
- Benefits of MSIs
- Low power management
- Configuration, initialization
- Enhanced error reporting

SERIAL RAPIDIO INTERFACE

- RapidIO port
- RapidIO doorbell and port-write unit
- Programming inbound and outbound ATMUs

SATA CONTROLLERS

- Support for SATA II extensions
- Bringing the SATA controller online/offline
- Native command queuing, command descriptor
- Interrupt coalescing
- Initialization steps

DATAPATH PROCESSING SUBSYSTEM

DPAA OVERVIEW

- Data formats
- Frame formats
- Packet walk through
- DPAA Configuration and initialization

QUEUE MANAGER

- Objectives if this accelerator
- Structure of frame queues
- Active and suspended frame queues
- Frame queue descriptor, frame queue descriptor cache
- Frame queue state machine
- Work queues and channels
- Enqueue and dequeue portals
- Utilization of rings
- Dequeue dispatcher operation
- Message ring
- Congestion avoidance, Weighted Random Early Discard
- Order definition point implementation

BUFFER MANAGER

- Objectives if this accelerator
- Central resource pool management function
- Per-pool stockpile
- CoreNET software portals
- Direct connect portals
- Buffer Pool State Change Notifications

FRAME MANAGER

- Objectives if this accelerator
- FMAN submodules
- Rx BMI features
- Tx BMI features
- Offline parsing, host command features
- Frame processing manager
- FMan controller
- Parser
- Key generator
- Policer

DATA PATH THREE-SPEED ETHERNET CONTROLLERS

- Frame format with and without VLAN option
- Connection to packet FIFO interface
- Physical interfaces
- 256-entry hash table for unicast and multicast
- Accessing PHY registers
- RMON statistic counters, carry registers
- Client IEEE1588 timers

10-GIGABIT MAC

- XAUI interface to PHY
- Multicast address filtering
- Dynamic inter packet gap (IPG) calculation
- MAC address insertion
- Support for VLAN
- IEEE 1588 timestamping

RAPIDIO MESSAGE MANAGER

- 2 inbox/outbox mailboxes (queues) for data and one doorbell message structure
- Multicasting
- Outbound segmentation units

RAID ENGINE

- Moving data, Scatter Gather List
- Chained command queue
- Non-DPAA descriptor Interface
- Data protection information
- IP checksum-based guard generation and checking

SECURITY ENGINE

- Introduction to DES, 3DES and AES algorithms
- Job management using QMan interface
- Input / output rings

- Cryptographic operations
- Data movement, FIFOs
- Scatter / gather DMA
- Selecting the authentication / cryptographic algorithm
- Run Time Integrity Checking
- Example, implementing IPSec

PATTERN MATCHER

- Objective of this unit, identifying signatures in incoming gigabit streams
- Connection to QMan and BMan
- Ability to track stateful relationships between patterns found in the data it scans
- Updating the pattern database
- Definition of a regular expression
- Comparing the string under inspection with the programmed patterns
- Processing pipeline, work units
- Pattern Matcher Frame Agent
- Pattern description block caching
- Key Element Scanner
- Data Examination Engine
- Stateful Rule Engine

GLOBAL FUNCTIONS, DEVELOPMENT AND DEBUG

PERFORMANCE MONITOR AND DEBUG FEATURES

- Introduction to NEXUS specification
- NEXUS Aurora link
- Event processing unit
- Watchpoint facility
- Trace buffer
- Event Combining for the Creation of Advanced Triggers
- Cross-Functional Debug Components
- DDR SDRAM interface debug, measuring per-master bandwidth

Renseignements pratiques

Durée : 6 jours
Prix : 3250 € HT