FCQ6 - P5020 QorIQ implementation

This course covers NXP QorIQ P5010 and P5020

Objectives

- This course has 6 main objectives:
  - Describing the hardware implementation, particularly the boot sequence and the DDR3 controller
  - Understanding the features of the internal interconnect and related units and mechanisms such as PAMU, CPC and stashing
  - Describing the units which are interconnected to other modules, such as clocking, interrupt controller and DMA controller, because the boot program generally has to modify the setting of these units
  - Explaining the standard bus interface controllers, PCIe, SRIO, USB and MMC-SD
  - Clarifying the operation of the Datapath Acceleration Architecture that assists the processor core in taking in charge buffer allocation, queue management, frame management and particularly incoming frame classification, pattern searching, and encryption
  - Describing the various debug units and their utilization to fix errors in a multicore / multimaster SoC.

- Products and services offered by ACSYS:
  - ACSYS is able to assist the customer by providing consultancies
  - Typical expertises are done during board bringup, hardware schematics review, software debugging, performance tuning.
  - Note that ACSYS has delivered several consultancies on NXP Netcomm SoCs to companies developing avionic equipments.

A more detailed course description is available on request at formation@ac6-formation.com
This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Pre-requisites

- Experience of a 32-bit processor or DSP is mandatory.
- Note that the e5500 Power core is covered in a separate course reference FCC2 - e5500 implementationcourse.

Related courses

- Ethernet and switching, reference N1 - Ethernet and switchingcourse
- IEEE1588, reference N2 - IEEE1588 - Precise Time Protocolcourse
- 10 Gigabit Ethernet, reference N3 - Ethernet 10 Gigabitcourse
- PCI express gen2, reference IC4 - PCI Express 3.0course
- RapidIO 2.1, reference IC5 - RapidIO 3.0course
- USB Full Speed High Speed and USB On-The-Go, reference IP2 - USB 2.0course
- SD / MMC, reference IS2 - eMMC 5.0course
- Serial-ATA, reference IS3 - Serial ATA IIIcourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

P5020 ARCHITECTURE

SOC ARCHITECTURE

- Block diagram
- Internal architecture
- CoreNet coherency fabric
- Coherency subdomains
- Memory map, local access windows
- Highlighting data paths inside the P5020, benefit of a dual-DDR controller system
- Application examples
- Multicore processing scenarios
- e5500 core integration

SOC PLATFORM

POWER, RESET AND CLOCKING

- Power management control
- Configuration signals sampled at reset
- Reset configuration words source
- Pre-boot loader
- Clocking, system clock domains
- Dynamically changing core clocks
- SerDes high speed lanes configuration

SECURE BOOT

- Objectives of trust architecture
- Secure boot sequence
- External tamper detection
- Run time integrity checker

CORENET PLATFORM CACHE

- Operation as memory-mapped SRAM
- Partitioning between coherency domains
- Stashing
- Soft error detection and correction

PERIPHERAL ACCESS MANAGEMENT UNIT (PAMU)

- Controlling master access permissions through Logical I/O Device Number
- Address translation
- Descriptor organization
- Operation mode translation
- Steps in processing of DSA operations by pamu
- PAMU caches

MULTIPROCESSOR PERIPHERAL INTERRUPT CONTROLLER

- Interrupt nesting
- Description of the 4 timers / counters
- Message interrupts
- e5500-to-e5500 interrupt capability

LOW SPEED PERIPHERALS

- UART
- I2C controller
- eSPI controller

ENHANCED SDHC

- Transfer protocol, single block, multiple block read and write
- Internal and external DMA capabilities
- SD protocol unit
- Card insertion and removal detection

USB CONTROLLERS

- Host or device support
- EHCI support, scheduling the various transactions into frames
- Integrated PHY
- Endpoint configuration
- Non-EHCI tuning control registers

HARDWARE IMPLEMENTATION

THE DDR3 / 3L MEMORY CONTROLLER

- DDR3 fly-by architecture, write leveling
- ZQ calibration
- Command truth table
- Hardware interface
- Initial configuration following Power-on-Reset
- Controller interleaving support
- Address decode unit
- Timing parameters programming

ENHANCED LOCAL BUS CONTROLLER

- Multiplexed or non-multiplexed address and data buses
- Connecting 8- and 16-bit devices
- Burst support
- GPCM, UPMs states machines
- NAND flash controller

INTEGRATED DMA CONTROLLERS

- Priority between the 4 channels
- Scatter / gathering
- Selectable hardware enforced coherency
- Ability to start DMA from external 3-pin interface

PCI EXPRESS INTERFACE

- Acting as a bridge when Root Complex
- Transaction ordering rules
- Programming inbound and outbound ATMUs
- Benefits of MSIs
- Low power management
- Configuration, initialization
- Enhanced error reporting

SERIAL RAPIDIO INTERFACE

- RapidIO port
- RapidIO doorbell and port-write unit
- Programming inbound and outbound ATMUs

SATA CONTROLLERS

- Support for SATA II extensions
- Bringing the SATA controller online/offline
- Native command queuing, command descriptor
- Interrupt coalescing
- Initialization steps

DATAPATH PROCESSING SUBSYSTEM

DPAA OVERVIEW

- Data formats
- Frame formats
- Packet walk through
- DPAA Configuration and initialization

QUEUE MANAGER

- Objectives if this accelerator
- Structure of frame queues
- Active and suspended frame queues
- Frame queue descriptor, frame queue descriptor cache
- Frame queue state machine
- Work queues and channels
- Enqueue and dequeue portals
- Utilization of rings
- Dequeue dispatcher operation
- Message ring
- Congestion avoidance, Weighted Random Early Discard
- Order definition point implementation

BUFFER MANAGER

- Objectives if this accelerator

- Central resource pool management function
- Per-pool stockpile
- CoreNET software portals
- Direct connect portals
- Buffer Pool State Change Notifications

FRAME MANAGER

- Objectives if this accelerator
- FMAN submodules
- Rx BMI features
- Tx BMI features
- Offline parsing, host command features
- Frame processing manager
- FMan controller
- Parser
- Key generator
- Policer

DATA PATH THREE-SPEED ETHERNET CONTROLLERS

- Frame format with and without VLAN option
- Connection to packet FIFO interface
- Physical interfaces
- 256-entry hash table for unicast and multicast
- Accessing PHY registers
- RMON statistic counters, carry registers
- Client IEEE1588 timers

10-GIGABIT MAC

- XAUI interface to PHY
- Multicast address filtering
- Dynamic inter packet gap (IPG) calculation
- MAC address insertion
- Support for VLAN
- IEEE 1588 timestamping

RAPIDIO MESSAGE MANAGER

- 2 inbox/outbox mailboxes (queues) for data and one doorbell message structure
- Multicasting
- Outbound segmentation units

RAID ENGINE

- Moving data, Scatter Gather List
- Chained command queue
- Non-DPAA descriptor Interface
- Data protection information
- IP checksum-based guard generation and checking

SECURITY ENGINE

- Introduction to DES, 3DES and AES algorithms
- Job management using QMan interface
- Input / output rings
- Cryptographic operations
- Data movement, FIFOs
- Scatter / gather DMA
- Selecting the authentication / cryptographic algorithm

- Run Time Integrity Checking
- Example, implementing IPSec

PATTERN MATCHER

- Objective of this unit, identifying signatures in incoming gigabit streams
- Connection to QMan and BMan
- Ability to track stateful relationships between patterns found in the data it scans
- Updating the pattern database
- Definition of a regular expression
- Comparing the string under inspection with the programmed patterns
- Processing pipeline, work units
- Pattern Matcher Frame Agent
- Pattern description block caching
- Key Element Scanner
- Data Examination Engine
- Stateful Rule Engine

GLOBAL FUNCTIONS, DEVELOPMENT AND DEBUG

PERFORMANCE MONITOR AND DEBUG FEATURES

- Introduction to NEXUS specification
- NEXUS Aurora link
- Event processing unit
- Watchpoint facility
- Trace buffer
- Event Combining for the Creation of Advanced Triggers
- Cross-Functional Debug Components
- DDR SDRAM interface debug, measuring per-master bandwidth

Renseignements pratiques

Duration : 6 days
Cost : 3250 € HT