FF1 - MCF5x07 implementation

This course covers MCF5307 and MCF5407 ColdFire MCUs

Objectives

- The course describes the ColdFire assembly language and highlights differences from 68K instructions.
- An example of SDRAM controller initialization is provided.
- Interfacing with external devices is explained.
- The interrupt controller is viewed in detail.
- Interrupt driven DMA transfers are studied.
- A programming example has been developped for each internal peripheral (serial; I2C, timer).

- This course has been delivered several times to companies developing industrial and avionics systems.

A lot of programming examples have been developed by ACSYS to explain the boot sequence and the operation of peripherals.
• They have been developed with Diab Data compiler and are executed under Lauterbach debugger.
A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

MCF5307 ARCHITECTURE

Overview

- Coldfire roadmap
- Differences between ColdFires and 68K processors
- 5307 block diagram
- Pinout
- Memory mapped I/O organization

V3 CORE

CORE ARCHITECTURE

- 5307 pipeline
- Programming model
- Addressing modes
- Instruction set
- Stack management, subroutine call and return
- C to assembly interface
- Exception management
- Internal SRAM
- 5307 cache operation

CORE DEBUG

- Intrusive vs non-intrusive debug
- BDM port
- Hardware breakpoints
- Trace port

PLATFORM

HARDWARE IMPLEMENTATION

- Dynamic bus sizing
- Address decoding
- Arbitration
- Burst cycles
- Bus error management

THE SIM MODULE

- The interrupt controller
- The software watchdog
- Reset, self-configuration
- Clock synthesis
- General Purpose I/O pins

THE MEMORY CONTROLLER AND THE DRAM/SDRAM CONTROLLER

- SRAM connection, chip-select programming

- DRAM / SDRAM basics
- The 5x07 (S)DRAM controller : address decoding, refresh rate definition, address multiplexing selection

INTEGRATED I/Os

THE SERIAL PORTS

- Asynchronous ports
- Transmit and receive sequences
- Synchronous port : I2C basics
- Transmit and receive sequences

THE DMA CONTROLLER

- Single address vs dual address transfers
- Hardware interface, hardware initiated transfers
- Programming model

THE TIMERS

- Capture mode
- Period selection
- Interrupt control

MCF5407 ENHANCEMENTS

MCF5407

- V4 core enhancements
- Instruction set additions
- Enhanced memories
- On-chip DMA and serial ports modifications

Renseignements pratiques

Duration : 4 days
Cost : 1950 € HT