FQ1 - LS1021A QorIQ implementation

This course covers the LayerScape LS1021A SoC

OBJECTIVES

- The course clarifies the architecture of the LS1021A, particularly the tuning of the interconnect.
- Cache coherency protocol is introduced in increasing depth.
- Only an overview of the ARM Cortex-A7 is provided, since this CPU is entirely covered by a separate course.
- The boot sequence and the clocking are explained.
- The course focuses on the hardware implementation of the LS1021A.
- A long introduction to DDR4 SDRAM operation is done before studying the DDR3L/DDR4 SDRAM controller.
- An in-depth description of the PCI-Express port is done.
- The course highlights both hardware and software implementation of gigabit / fast / Ethernet controllers .
- Communication interfaces are explained including QuiccEngine.

- This course is only delivered on site and therefore its contents can be adapted to specific customer needs from the outlines described hereafter.

A more detailed course description is available on request at training@ac6-training.com

PREREQUISITES AND RELATED COURSES

- Experience of a 32-bit processor or DSP is mandatory.
- Knowledge of PCI Express bus is recommended.

- This course provides only an overview of the Cortex-A7.
- Our course reference RA4 - Cortex-A7 implementationcourse details the operation of this complex ARM CPU.
- Our course reference RC1 - NEON-v7 programmingcourse explains how to vectorize and implement algorithms to be executed by NEON SIMD engine.

- The following courses could be of interest:
  - USB Full Speed High Speed and USB On-The-Go, reference IP2 - USB 2.0course
  - USB Super Speed, reference IP3 - USB 3.0course
  - Ethernet and switching, reference N1 - Ethernet and switchingcourse
  - IEEE1588, reference N2 - IEEE1588 - Precise Time Protocolcourse
  - CAN bus, reference IA1 - CAN buscourse
  - Memory cards, reference IS2 - eMMC 5.0course
  - SATA, reference IS3 - Serial ATA IIIcourse
  - PCI Express, reference IC4 - PCI Express 3.0course

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION TO LS1021A

BLOCK DIAGRAM

- SoC architecture
- Fixed memory map
- Local vs external address spaces, inbound and outbound address decoding

INTERCONNECT

- CCI-400, Cache Coherent switch fabric
- AMBA 4 snoop request transport
- Snoop connectivity and control
- Ensuring data coherency of I/O streams through ACE-Lite ports
- System MMU
- Programming the TrustZone firewall
- OCRAM controller
- QoS tuning

THE CORTEX-A7 CPUs

OVERVIEW OF CORTEX-A7

- Cortex-A7 architecture
- 64-Byte cacheline size, integrated L2 cache
- VFPv4 and SIMDv2
- Instruction pipeline

TRUSTZONE

- TrustZone conceptual view
- Secure to non secure permitted transitions
- L1 and L2 secure state indicators, memory partitioning
- System security, Central Security Unit
- Secure Non Volatile Storage

EXCEPTION MECHANISM

- V7-A exception mechanism

- GICv2

LARGE PHYSICAL ADDRESS EXTENSIONS SPECIFICATION (LPAE)

- Need to introduce support for a second stage of translation as part of the Virtualization Extensions
- New 3-level system
- Hypervisor-level address translation
- Level-1 table descriptor format
- Level-2 table descriptor format
- Attribute and Permission fields in the translation tables
- Complete set of cache allocation hints
- Handling of the ASID in the LPAE

LEVEL ONE SUBSYSTEM

- Cache organization, 2-way instruction cache, 4-way data cache
- Pseudo random replacement algorithm
- Speculative accesses
- Hit Under Miss, Miss under Miss
- Detailing cache maintenance operations

LEVEL TWO SUBSYSTEM

- L2 Cache
- Read allocate mode
- ACE master interface
- By means of sequences involving a multi-core Cortex-A7 and external masters, understanding how snoop requests can be used to maintain coherency of data between caches and memory

INFRASTRUCTURE

RESET, CLOCKING AND INITIALIZATION

- Clock subsystem block diagram
- Reference clock for SerDes protocols
- Voltage configuration selection
- Power-on reset sequence, detailing Reset Configuration Words
- Power-on reset configuration
- Pre-Boot Loader, required format of data structure consumed by PBL
- Boot from parallel flash: NOR and NAND
- Boot from serial flash: eSDHC and QuadSPI
- Watchdog timer

SECURE BOOT AND TRUST ARCHITECTURE

- Objectives of trust architecture
- Internal boot ROM, secure boot sequence
- Security fuse processor
- Code signing
- External tamper detection
- Run time integrity checker
- Key revocation

RUN CONTROL AND POWER MANAGEMENT

- Software-controlled power management states
- Core power management, doze and nap states
- Device power management, sleep and deep-sleep states
- Wake-up sources

SERDES MODULE

- Interfaces from 1.25 to 6 Gbps
- External Signals Description
- SerDes Lane Assignments and Multiplexing
- SerDes clocking

DDR3L/DDR4 SDRAM MEMORY CONTROLLER

- DDR3L and DDR4 Jedec specification
- DDR4 new features: Pseudo Open Drain termination, bank groups
- Calibration mechanism
- Command truth table
- Hardware interface
- Bank activation, read, write and precharge timing diagrams, page mode
- ECC error correction
- Freescale DDR 3/4 controller
- Initial configuration following Power-on-Reset

INTEGRATED FLASH CONTROLLER

- Functional muxing of pins between NAND, NOR, and GPCM
- Normal GPCM FSM
- Flexible timing control
- NOR flash FSM
- Generic ASIC FSM
- NAND flash FSM
- ONFI-2.2 asynchronous interface
- ECC generation/checking
- SLC and MLC Flash devices support with configurable page sizes
- Internal SRAM of 9 KByte

PCI EXPRESS INTERFACE

- 4-lane PCI Express interface
- Modes of operation, Root Complex / Endpoint
- Transaction ordering rules
- Programming inbound and outbound ATMUs
- MSI management
- Configuration, initialization

QUAD SPI

- External signal description
- Interface to one single or two external serial flash devices
- Programmable sequence engine
- AHB buffers, Look Up Table
- Memory mapped read access to connected flash devices
- Flash programming

INTEGRATED CONTROLLERS

- eDMA
- qDMA

SATA3 CONTROLLER

- SATA basics
- Electrical specification
- AHCI command layerStandard ATA master-only emulation

- Command list structure
- Interrupt coalescing
- FIS-based switching

SECURITY ENGINE

- Introduction to DES, 3DES and AES algorithms
- Job descriptor parsing
- Sharing descriptors
- Data movement, FIFOs
- Scatter / gather DMA
- Selecting the authentication / cryptographic algorithm
- Export and Import of cryptographic Blobs
- Public Key Hardware Accelerator (PKHA)
- SNOW 3G Accelerator
- Data Encryption Standard Accelerator (DES)
- Cyclic Redundancy Check Accelerator (CRCA)
- Message Digest Hardware Accelerator (MDHA)
- Elliptic Curve Cryptographic Functions

INPUTS/OUTPUTS

COMMUNICATION INTERFACES

- Ethernet Controllers
  - 802.3 specification fundamentals
  - Address recognition, pattern matching
  - Physical interfaces
  - Layer 2 acceleration accept or reject on address or pattern match
  - Management of VLAN tags and priority, VLAN insertion and deletion
  - Quality of service, managing several transmit and receive queues
  - TCP/IP offload engine, filer programming
  - IEEE1588 compliant time-stamping
  - Interrupt coalescing
- UARTs
- I2C
- SPI
- FlexCAN controllers

ENHANCED SECURE DEVICE HOST CONTROLLER

- Introduction to MMC and SD card
- Storing and executing commands targeting the external card
- Multi-block transfers
- Read transfer sequence
- Write transfer sequence

USB CONTROLLERS

- USB 2.0 controller
- USB 3.0 controller

MULTIMEDIA INTERFACES

- Display interface unit
- SSI interfaces
- Asynchronous Sample Rate Converter
- SPDIF receiver / transmitter

FLEXTIMER MODULE

- 16-bit timer modes, up-counter, down-counter,
- Input capture
- Output compare
- PWM

QUICC ENGINE

OVERVIEW OF QUICC ENGINE

- Communication between Host ARM CPU and QE RISC CPU, utilization of Command Register
- Mapping of integrated resources

INTEGRATED INTERRUPT CONTROLLER

- Priority management, understanding the priority table
- Managing the priority within priority groups and between priority groups
- Steering the interrupt source to either Low priority or High priority input of the platform PIC

SYSTEM INTERFACE AND CONNECTION TO EXTERNAL COMMUNICATION PORTS

- Serial DMA
- NMSI vs TDM
- Enabling connections to TSA or NMSI
- CMX registers

BUFFER MANAGEMENT

- Utilization of Buffer Descriptors
- Chaining descriptors into rings
- Interrupt management

UNIFIED COMMUNICATION CONTROLLERS

- Handling UCC interrupts
- Initialization sequence
- Defining Tx- and Rx-FIFO thresholds

UCC HDLC CONTROLLER

- HDLC frame description
- Flow control
- Host commands

UCC TRANSPARENT CONTROLLER

- Transparent data encapsulation, frame sync and frame CRC
- Flow control
- Host commands

SERIAL INTERFACE

- Connecting TDM lines
- Parameterizing the timings related to Rx/Tx clock, sync and data signals

MULTI-CHANNEL CONTROLLER ON UCC - UMCC

- Clarifying the various tables that must be implemented in MURAM
- Connecting time-slots to logical channels through Rx/Tx routing tables
- Implementing Rx/Tx channel buffers
- Interrupt management, benefits of interrupt queues
- Modes of operation, transparent, HDLC

Renseignements pratiques

Duration : **5 days**
Cost : **2930 € HT**