# ac6

## FA3 - i.MX51 Implementation + LTIB

## This course describes the i.MX51 multimedia processor and Linux Target Image Builder tool

### Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- Practical activities
  - Practical activities represent from 40% to 50% of course duration.
  - Code examples, exercises and solutions
  - For remote trainings:
    - One Online Linux PC per trainee for the practical activities.
    - The trainer has access to trainees' Online PCs for technical and pedagogical assistance.
    - QEMU Emulated board or physical board connected to the online PC (depending on the course).
    - Some Labs may be completed between sessions and are checked by the trainer on the next session.
  - For face-to-face trainings:
    - One PC (Linux ou Windows) for the practical activities with, if appropriate, a target board.
    - One PC for two trainees when there are more than 6 trainees.
  - For onsite trainings:
    - An installation and test manual is provided to allow preinstallation of the needed software.
    - The trainer come with target boards if needed during the practical activities (and bring them back at the end of the course).
- Downloadable preconfigured virtual machine for post-course practical activities
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

### Prerequisites

- Knowledge of ARM architecture is recommended
- Knowledge of Linux basics is recommended

### Documentation

- Training manuals will be given to attendees during training both in pdf and in print. Precise and easy to use, those notes can be used as a reference afterwards.

### Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

### Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed in two different ways, depending on the course:

- o For courses lending themselves to practical exercises, the results of the exercises are checked by the trainer while, if necessary, helping trainees to carry them out by providing additional details.
- o Quizzes are offered at the end of sections that do not include practical exercises to verifythat the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - o In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

## Plan

### Architecture of MCIMX51

- Clarifying the internal data paths : AXI interconnect, AHB bus, peripheral buses
- Highlighting the purpose of the 2 central interconnect units : MAX and M4IF
- Organization of a board based on MCIMX51
- Mapping

### The ARM Cortex/A8 Core - Overview

- Operating modes : user, system, super, IRQ, FIQ, undef and abort
- ARM vs Thumb-2 instruction sets, interworking
- Access to memory-mapped locations, addressing modes
- Stack management
- Branch instructions, implementation of C call and return statements
- Level1 cache operation
- Level2 cache operation
- Memory management unit, TLB
- C-to-Assembly interface
- Exception mechanism, handler table

### Reset and Clocking

- Clock distribution
- DVFS support
- Power Gating Controller
- Low power modes, wake-up detector
- Global reset vs warm reset
- System boot mode selection
- eFUSE configuration

### System Control

- GPIO module
- General Purpose Input interrupt request capability

### The Cortex/A8 Platform

- MAX parameterizing
- ARM Vector Interrupt Controller
- Integrated timers EPIT, GPT, WDT

### Debug Architecture

- Introduction to CoreSight, DAP features
- System Secure Controller SJC
- Embedded Trace Macrocell
- Cross Triggering Interfaces

## Smart DMA Controller

- Mapping DMA requests to channels
- Channel priority definition
- Scheduler
- Instruction description
- PCU states
- Context switching
- Reference clocks and low power modes
- Debug support
- Profiling unit

## Accessing External Memories

- Description of the Master Arbitration and Buffering [MAB] unit
- Description of the M4IF arbitration [M3A] unit
- Introduction to DDR2/LPDDR SDRAM
- Enhanced DDR2 SDRAM controller
- NAND flash controller, boot from flash

## System Security

- Security Controller
  - Protecting information and data from unauthorized access
  - A dedicated AES cryptographic engine
  - High Assurance Boot
- SAHARA4 security coprocessor
  - Random number generator
  - Encryption / decryption sequences
  - Restricted access to potentially sensitive information
  - ARM TrustZone support
- Run-Time Integrity Checker
  - SHA-1 and SHA-256 message authentication
  - Segmented data gathering
  - One-time hash mode vs continuous hash mode
- IC Identification Module

## Standard Parrallel Interfaces

- ATA controller
  - Pinout
  - PIO mode
  - Ultra DMA mode
- Enhanced SDHC
  - Interface to SD, MMC, SDIO and CE-ATA cards
  - Transfer protocol, single block, multiple block read and write
  - Internal and external DMA capabilities
  - Error management

## Video Processing Units

- Video Processing Unit
  - Codec hardware
  - Encoding pipeline
  - Video Codec processing buffer requirement
- Image Processing Unit v3
  - Video acquisition
  - Image Signal Processor, processing captured images
  - Processing chain description
  - Display processor, processing chain

- o Video de-interlacer
- o Image converter
- o Image rotator
- o Display port
- Graphics Processing Unit 2D
  - o 2D bitmap graphics
  - o Vector graphics
  - o Connection to DMA controller
- Graphics Processing Unit 3D
  - o Sophisticated shader support
  - o Graphics core
  - o Graphics memory
  - o Pixel blender
  - o Integrated MMU
- TV encoder
  - o Supported TV standards, SD/HD modes
  - o TV signal processor
  - o Cable detection circuit

## Audio Related Interfaces

- SSI interfaces
  - o Connection of Codecs or DSPs
  - o I2S mode
  - o AC97 support
- Digital audio multiplexor
  - o Connecting host interfaces to peripheral interfaces
  - o Internal network mode
- SPDIF transmitter
  - o Selecting the clock
  - o Transmit FIFO operation

## Communication Controllers

- 1-wire interface
- Configurable SPI, enhanced CSPI
  - o SPI protocol basics
  - o Transfer sequence
- High Speed I2C and I2C interfaces
  - o I2C protocol basics
  - o Transfer sequence
- Fast Infrared Interface [FIRI]
  - o MIR packet structure, MIR modulation
  - o FIR packet structure, FIR modulation
- UART
  - o Individual baud rate generators
  - o Flow control
- USB
  - o Explaining what is OTG
  - o The 3 USB ports
  - o High-speed operation
  - o EHCI support
  - o ULPI bypass mode
- Fast Ethernet Controller [FEC]
  - o Ethernet basics
  - o Incoming frame filtering mechanisms, hash tables
  - o Flow control in Full Duplex mode
  - o VLAN support
- SIM
  - o Introduction to IEC / ISO 7816

  ○ Transferring packets

## Generating the Linux Kernel Image

- Introducing the tools required to generate the kernel image
- What is required on the host before installing LTIB
- Common package selection screen
- Common target system configuration screen
- Building a complete BSP with the default configurations
- Creating a Root File Systems image
- Re-configuring the kernel under LTIB
- Selecting user-space packages
- Setup the bootloader arguments to use the exported RFS
- Debugging Uboot and the kernel by using Trace32
- Command line options
- Adding a new package
- Other deployment methods
- Creating a new package and integrating it into LTIB

*Exercise: Several labs will help explain the usage of LTIB*

## Renseignements pratiques

**Duration :  5 days**
**Cost :  1950 € HT**