V0 - Programmable components fundamentals

This training is intended to professional who want to use or maintain programmable components

Objectives

- Knowing the programmable logic basics
- Knowing the general offer for CPLDs and FPGAs
- Understand application description in HDL
- Understand the logical synthesis notions and process flow
- Discover FPGA programming in VHDL and Verilog
- Understand how to elaborate and simulate a design

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- Practical activities
  - Practical activities represent from 40% to 50% of course duration.
  - Code examples, exercises and solutions
  - For remote trainings:
    - One Online Linux PC per trainee for the practical activities.
    - The trainer has access to trainees' Online PCs for technical and pedagogical assistance.
    - QEMU Emulated board or physical board connected to the online PC (depending on the course).
    - Some Labs may be completed between sessions and are checked by the trainer on the next session.
  - For face-to-face trainings:
    - One PC (Linux ou Windows) for the practical activities with, if appropriate, a target board.
    - One PC for two trainees when there are more than 6 trainees.
  - For onsite trainings:
    - An installation and test manual is provided to allow preinstallation of the needed software.
    - The trainer come with target boards if needed during the practical activities (and bring them back at the end of the course).
- Downloadable preconfigured virtual machine for post-course practical activities
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Prerequisites

- Knowledge of digital technology
- Concepts of Boolean algebra
- Some programming concepts are desirable (whatever language)

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed in two different ways, depending on the course:
  - For courses lending themselves to practical exercises, the results of the exercises are checked by the trainer while, if necessary, helping trainees to carry them out by providing additional details.
  - Quizzes are offered at the end of sections that do not include practical exercises to verifythat the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

First Day

From the logic gate to the CPLDs and FPGAs

- Reminder on digital electronic
- Structure of an Integrated Circuit
- SSI (small scale integration), TTL
- MSI (medium scale integration), PALs, GALs, PLDs
- LSI (large scale integration), CPLDs
- VLSI (very large scale integration), ASICs, ASSPs, FPGAs
- Logical architectures evolution
- The various components
- Technologies available on the market
- Technology constraints
- Interconnection methods (SRAM, Fuse, AntiFuse, Flash)
- Clock distribution
- Logic element types
- Timing issues

HDL Contribution

- Interest of HDL programming
  - VHDL
  - Verilog
- Different steps of the design
  - Programming
  - Simulation
  - Synthesis
  - Mapping
  - Place and Route
  - Timing Analysis
  - Bitstream generation
- Definition of a project
- Structure of a program
- Allocation of PIN-OUT
- Programming

Exercise: *Understanding the steps of design and programming:*

- *Getting started with the ISE IDE*
- *Creating a project from scratch*
- *Synthesis, Translate*
- *Map*
- *Place and Route (PAR)*
- *BitGen*
- *Report Analysis*
- *Assigning I/O locations using Planahead (editing constraint file)*
- *Schematics*
- *Analyzing the placement*
- *Flashing with Impact*

Second Day

Schematic Editor

- The schematic capture
- Primitives and symbols definition
- Resources definition
- Compilation

Exercise: *Developing a new IP with the Schematic Editor, Designing a Bound Detector*

HDL Basic Concepts (VHDL and Verilog)

- Entity/ Architecture and Module
- Signals and wires
- Processes and Always/Initial statements
- Connecting existing IPs together

Exercise: *Adding a 7-Segment Display to your design*

Test benches and simulation

- HDL instructions specific to simulation
- Functional and behavioral simulation (with delays)
- Test vector generation

Exercise: *Getting started with the ISIM simulator, developing a tesbench and simulating the previous designs*

Renseignements pratiques

Duration : 2 days
Cost : 2070 € HT