HX1 - Xilinx - Virtex-5 FXT Embedded Processor Block

This course covers the parameterizing of the Embedded Processor Block present in Virtex-5 FXT Xilinx FPGAs.

Objectives

- This course describes in depth the PPC440 core, including the optional FPU.
- Differences between PPC440 and PPC405 are highlighted.
- Practical labs provide CPU performance estimations through fixed-point and floating-point FFTs.
- The course also details the operation of the internal crossbar connecting the PPC440, external PLB masters, LocalLink DMA channels to PLB slaves and memory.
- The address decoding logic and arbitration mechanisms are explained through the EDK embedded processor block parameterizing wizard.
- The LocalLink protocol is studied in order to clarify how data are transferred between hard LocalLink DMA channels and external soft IPs.
- The course focuses on error recovery mechanisms that can be used during debug time to understand and fix bus errors.

- This course has been designed by processor experts from Ac6, developing courses for IBM Microelectronics and AMCC for more than 10 years.

A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

PPC440x5 CORE, HIGHLIGHTING DIFFERENCES WITH PPC405

- 7-stage pipeline operation, dual issue superscalar pipeline
- Speculative execution, guarded memory
- Serialization
- Caches, 64-way associativity, cache line locking
- Using a part of the cache to store transient information
- Clarifying the instruction and data path
- Cache programming interface
- Memory Management Unit
- Translation Lookaside Buffer initialisation
- Load / store buffer, speculative loads, msync and mbar instructions
- Floating Point Unit (external soft IP), compliance with IEEE754
- Float MAC instructions
- Interrupt management
- Reset clock and power management interfaces
- Debug interfaces : JTAG and trace

CORE BUS INTERFACES

- Architecture of a SOC designed with Virtex-5 FXT, hard IPs vs soft IPs
- DCR controller, direct addressing vs indirect addressing
- Dual DCR master arbitration
- Detailing the difference between PLB4 and PLB3
- Transaction types : single data, line, burst
- Connecting a coprocessor to the APU 128-bit load/store interface
- Concurrent operation with the core pipeline
- Detail of the interface between APU controller and Fabric Coprocessor Module
- FCM user-defined instructions
- Exception management

INTERNAL CROSSBAR

- Block diagram (Muxes and demuxes)
- 5 PLB slave interfaces, 3 for the core + 2 for soft PLB masters
- 4 full-duplex LocalLink channels with built-in DMA control
- 1 high-speed memory controller interface
- 1 master interface to connect an external slave soft IP
- Issues with transaction ordering, sync attribute, specification configuration to support PCI/PCIe
- Describing the various arbitration algorithms
- Error management, error syndrome registers, related interrupts

DMA CONTROLLER

- Scatter / gather operation, direct mode vs chained mode
- Setting the channel priority
- Asynchronous interface to LocalLink soft IP
- Interrupt mechanism, coalescing
- Dynamic descriptor appending
- Software / device driver considerations

MEMORY CONTROLLER

- Generation of intermediate addresses during bursts
- Constant burst length set by the user through a control register
- Row and bank detect logic

- ECC management
- Implementing the Xilinx DDR2 memory controller

PARAMETERIZING THE EMBEDDED PROCESSOR BLOCK

- Static configuration through attributes
- Dynamic reconfiguration through DCRs
- Crossbar configuration
- DMA channel configuration
- Generating the platform by using PlatGen

Renseignements pratiques

Duration : 3 days
Cost : 1950 € HT