IA1 - CAN bus

This course covers all CAN specifications: CAN 2.0, TT-CAN and FD-CAN

Objectives

- Becoming familiar with CAN 2A & 2B specifications through implementation examples.
- Explaining the benefits and implementation of TT-CAN.
- Highlighting the differences between CAN 2.0 and FD-CAN.
- Describing the M-TTCAN IP designed by Bosch, as an implementation example of the CAN 2.0, TT-CAN and FD-CAN specifications.
- This course also details the physical layer.
- Testing a CAN system and optimising the hardware parameters with the assistance of a IXXAT CAN Analyser.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Basic knowledge of processor.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION

- History

- Compliance with the OSI model
- PHY and Link layers features

FRAME ANALYSIS

- 2.0A and 2.0B frame description
- Compatibility between both formats
- Relationship between label and priority

ARBITRATION

- Point to multipoint communication model
- Dominant and recessive states
- Frame priority selection through the label value

TIMING AND SYNCHRONIZATION

- Bit time phases
- Hardware and software resynchronization
- RJW determination

ERROR MANAGEMENT

- The error counter registers
- Error detection areas inside a transmit frame and a receive frame
- Fault confinement : counter increment / decrement rules
- The 3 states of a CAN node

CAN NETWORK PERFORMANCE

- The parameters that determine network performance
- Distance between both farthest stations
- Connection establishment time

SETTING UP A CAN BUS SYSTEM

- Set up of many communications between all CAN stations
- Labs to show the error counter management
- Labs to show the impact of the RJW parameter

CAN SOFTWARE DRIVER DEVELOPMENT

- STM32 CAN controller description
- Label filters configuration through the mask registers
- Bit time phases initialization
- Automatique reply

TIME-TRIGGERED CAN

- Transmitting messages in specific time slots
- System matrix, time windows
- Frame synchronisation entity, global system time
- Merged arbitrating windows
- Reference message
- Generation of Local time
- Initialisation and fault tolerance of time masters
- Failure handling
- Interrupt status vector
- Message status count

CAN WITH FLEXIBLE DATA RATE (FD-CAN)

- Two bit-rate scheme
- New MAC and LLC layers
- New frame format
- Extended Data Length, up to 64 Bytes
- Bit Rate Switch
- Error State Indicator

M_TTCAN BOSCH IP

- Clocking
- Power-down support
- Message RAM organization
- RxBuffer and TxBuffer elements
- Parameterizing the frame filters
- Interrupt management
- Loopback test mode
- Bus monitoring mode
- Programming, describing control and status registers
- Monitoring the CAN communication state
- Activating FD operation
- TT synchronization state
- Cycle time, Global time and Local time
- Message scheduling

Renseignements pratiques

Duration : 2 days
Cost : 1970 € HT