AT1 - AT91SAM7SE microcontroller implementation

This course covers AT91SAM7SE ARM based microcontroller

Objectives

- The course details the hardware implementation of the AT91SAM7 microcontrollers.
- The boot sequence and the clocking are explained.
- Practical lab on integrated peripherals are based on I/O functions provided by Atmel.
- The course focuses on the low level programming of the ARM7TDMI core.
- The course provides examples of internal peripheral software drivers.

- Note that ACSYS does not sell emulation probes and IDEs. Consequently this course has not been designed to convince attendees to buy a particular IDE. The unique objective consists in providing sufficient knowledge to attendees so that they can successfully design a system based on AT91SAM7.

- This course has been delivered several times to companies developing embedded systems, such as badges and RF equipments.

A lot of programming examples have been developed by ACSYS to explain the boot sequence, the vector table and the operation of embedded peripherals.

- *They have been developed with 2 different IDEs : Keil and IAR.*
- *Consequently for on site course, it is up to the customer to select the IDE under which labs will be run.*

A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites and related courses

- This course provides an overview of the ARM7TDMI core. Our course reference R1 - ARM7/9 implementationcourse details the operation of this core.
- The following course could be of interest:
  - USB Full Speed High Speed and USB On-The-Go, reference IP2 - USB 2.0course

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.

- In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION TO AT91SAM7

Overview

- ARM core based architecture
- APB internal busses
- The main three blocks : platform, core and input / output peripherals

THE PROCESSOR CORE

THE ARM7TDMI CORE

- Operating modes
- ALU data path
- ARM vs Thumb instruction sets, interworking
- Access to memory-mapped locations
- Stack management
- Benefits of condition set capability in ARM state
- C-to-Assembly interface
- Exception mechanism, handler table

PLATFORM

INFRASTRUCTURE

- Power supplies, internal regulator
- Clock generator
- Reset controller
- SAM-BA default boot program
- Memory controller
- Internal high-speed flash
- External Bus Interface
- Power management controller
- Advanced interrupt controller
- Parallel input / output controller
- Peripheral DMA controller

INTEGRATED I/Os

NON COMMUNICATION ORIENTED INPUT / OUTPUT PERIPHERALS

- Timers
  - Periodic Interval Timer
  - Windowed Watchdog
  - Real-time timer
  - 3-channel timer / counter
  - 16-bit PWM controller
- Analog-to-Digital Converter

- 8-channel 10-bit ADC
- Conversion trigger
- ADC timings

COMMUNICATION CONTROLLERS

- 2-wire interface
  - I2C protocol basics
  - Transmit and receive sequences
- SPI
  - SPI protocol basics
  - External chip-select
  - Transfer sequence
- USART
  - Individual baud rate generators
  - IrDA modulation / demodulation
  - Support for Smart Card
  - RS485 support
- Synchronous Serial Controller
  - I2S analog interface support
  - Time Division Multiplexed support
  - High speed continuous data stream capabilities
- USB
  - Full speed operation
  - Endpoint configuration

Renseignements pratiques

Duration : 4 days
Cost : 2000 € HT