R2 - ARM11 implementation

This course covers ARM1136 and ARM1176 CPUs

Objectives

- This course is split into 3 important parts:
  - ARM11 architecture
  - ARM11 software implementation and debug
  - ARM11 hardware implementation.
- MMU operation under Linux is described.
- Interaction between level 1 caches, level 2 cache and main memory is studied through sequences.
- The exception mechanism is detailed, particularly the utilization of the VIC port.
- The course also details the hardware implementation and provides some guidelines to design a SoC based on ARM1136/76.
- An overview of the Coresight specification is provided prior to describing the debug related units.
- ACSYS has developed FFTs optimized for ARM11 coded in assembler language
  - performance for 1024 complex floating point single precision samples is 220_000 core clock cycles for VFP11 (ARM11)
  - performance for 1024 complex fixed point 16-bit samples is 206_000 core clock cycles (ARM SIMD V6 instructions)
  - for any information contact formation@ac6-formation.com

Labs are run under RVDS

A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites

- Knowledge of ARM7/9 or having attended the ARM fundamentals course.
- This course does not include chapters on low level programming.
  - ACSYS offers a large set of tutorials to become familiar with RVDS, assembly level programming, compiler hints and tips.
- More than 12 correct answers to ARM11 prerequisites questionnaire.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- **The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.**
- **Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented**
- **At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.**
  - **In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.**

Plan

First day

ARM BASICS

- **States and modes**
- **Exception mechanism**
- **Instruction sets**
- **Purpose of CP15**

INTRODUCTION TO ARM1136JF-2 AND ARM1176JZF-S

- **Block diagram**
- **Highlighting the instruction path and the data path**
- **Clarifying the usage of the 4 AHB / AXI ports**
- **Typical architecture of a SoC based on ARM1136/76**

ARM11 CORE PIPELINE

- **Pipeline stages**
- **Branch prediction**
- **Return stack**
- **Instruction memory barrier, use case**

TRUSTZONE

- **Objectives**
- **Clarifying the transitions between NS OS Secure Monitor Secure OS**
- **Consequences on caches and TLBs**
- **Secure boot, boot sequence**
- **Distinguishing the Secure vector table from the NS vector table**
- **Enabling / disabling invasive and non-invasive secure debug**

V6 MMU

- **Memory types**
- **Inner and outer cache attributes**
- **Data memory barrier, data synchronization barrier, use cases**
- **Objectives of the MMU**
- **Page descriptors**
- **Highlighting the new features of the V6 architecture regarding the MMU**
- **Locking entries in TLB**
- **Abort status, imprecise abort**

Second day

LEVEL 1 CACHES

- **Cache basics**
- **4-way set associative caches, virtual indexing, page coloring**
- **Hit under miss capability**
- **Maintenance operations**

TCM AND DMA CHANNELS

- **TCM, address decoding**
- **DMA channels**
- **DMA state machine, interrupts**
- **DMA programming, using virtual addresses**

AHB PROTOCOL (ARM1136 specific, on request)

- **Centralized address decoding**
- **Address gating logic**
- **Arbitration, bus parking**
- **Address pipelining**
- **Retry response**
- **Split response**

AXI PROTOCOL

- **AMBA 3**
- **AXI protocol, the 5 communication channels**
- **Channel handshake mechanism**
- **Basic transactions, read burst, write burst**
- **Protection attributes**
- **Data buses, utilization of byte write strobes**
- **Unaligned transfers**
- **Response signalling, requirement of a default slave**
- **Atomic access, exclusive vs locked transfers**
- **ARMv6 load / store exclusive instructions**
- **Ordering model**
- **Slave parameters**
- **AXI interconnection architectures**

HARDWARE IMPLEMENTATION

- **Reset sequence, power on reset and warm reset timing diagrams**
- **Power management, run, standby and shutdown modes**
- **New dormant mode**
- **Interface to power manager**

Third day

L220 / L210 CACHE

- **Indicating the purpose of internal buffers**
- **Write allocate policies**
- **Write merging**
- **Event monitoring**
- **Cache maintenance operations**

- **Low power interface**
- **Register block**

EXCEPTION MANAGEMENT

- **The 3 interrupt controller models: simple controller, vectored controller and controller using the VIC port**
- **Benefit of the VIC port interface**
- **New feature regarding exceptions: low latency mode**

ARM11 DEBUG

- **Performance monitor**
- **Instruction breakpoints and data watchpoints**
- **Vector catch hardware**
- **Thread aware debug**
- **Halt mode vs monitor mode**
- **Debug communication channel**

ARM11 REAL-TIME TRACE

- **Coresight ETM11**
- **AMBA Trace Bus, trace port and Embedded Trace Buffer**
- **Instruction tracing**
- **Data tracing**
- **Programming ETM11CS**

Renseignements pratiques

Duration : 3 days
Cost : 1650 € HT