M7 - 440SPe implementation

This course covers AMCC 440SPe processor

Objectives

- The course explains how to design a 440SPe board, highlighting reset and clocking.
- The data flows between PCI-X, PCI Express and DDR SDRAM are described.
- The course explains how to configure the internal buses (PLB crossbar and PLB-to-OPB bridge).
- DDR SDRAM operation is described in order to understand both the electrical interface and the memory controller programming.
- Book E PowerPC architecture is studied, especially the MMU.
- The course provides examples of internal peripherals software drivers.
- Gigabit Ethernet controller is viewed in detail.

- A chapter on Linux porting can be appended on request.

Labs are compiled with Diab Data compiler and run under Lauterbach debugger.
A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.
- Knowledge of PCI-X bus is recommended, see our course reference IC3 - PCI-X 2.0course.
- Knowledge of PCI Express bus is recommended, see our course reference IC4 - PCI Express 3.0course.
- Knowledge of Gigabit Ethernet is recommended, see our course reference N1 - Ethernet and switchingcourse.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION TO 440SPe

- Block diagram
- Internal bus organization : dual PLB, OPB, DCR
- Internal concurrent transfers examples
- Introduction to Integrated peripherals
- Hardware implementation
- 440SPe memory mapping
- Programming model

ON CHIP BUSES

- Introduction to CoreConnect
- 2-way PLB crossbar, programming
- Bus errors recovery from syndrome registers
- PLB performance monitor

440 CORE

- Pipeline
- Internal caches
- Speculative loads, storage ordering and synchronization : msync & mbar instructions
- MMU

BOOK E COMPLIANT CORE

- Programming model
- Branch instructions
- Addressing modes, load & store instructions
- Integer instructions
- 16-bit mac instructions to develop DSP algorithms
- Exception management
- Exception priorities
- Core timers
- PowerPC EABI
- JTAG debug
- Real time trace

CLOCKS, RESET AND POWER MANAGEMENT

- Clocks synthesizer
- PCI-X clocking
- PCI Express clocking
- Clock and power management
- Low power modes
- Reset signals
- Initialization software requirements
- IIC bootstrap controller : processor configuration through the IIC port
- PCI-X bootstrap configuration
- Peripheral software reset
- Booting from local ROM in Host bridge mode
- Booting from local ROM in Agent bridge mode
- Booting from PCI

L2 CACHE CONTROLLER & INTERNAL SRAM CONTROLLER

- L2 cache features
- Data movement between memory, L2 and L1 caches
- L2 cache programming
- SRAM controller

INTERRUPT CONTROLLER & GENERAL PURPOSE TIMERS

- Interrupt masking and acknowledgement sequences
- Critical interrupt handlers using vectorization
- Interrupts priority management
- General Purpose Timers

THE DDR-SDRAM CONTROLLER

- DDR-SDRAM operation
- Jedec specification basics
- Hardware interface, SSTL-2 termination logic
- Differences between DDR-I and DDR-II
- ECC error correction
- Introduction to the 440SPe DDR-SDRAM controller
- Page management unit
- Initialization sequence
- Hardware implementation

THE EXTERNAL BUS CONTROLLER

- External bus pinout, driver enables
- Dynamic bus sizing
- Timing parameters
- Device-paced transfers

THE PCI-X BUS CONTROLLER

- DDR PCI-X operation
- Host vs agent configuration
- Data flows : Read prefetch and write posting buffers
- Inbound transactions handling, Outbound transactions handling
- Error handling
- Arbitration algorithm
- Boot modes, initialization / Reset sequence
- Sleep mode entering
- PCI-Express to PCI-X bridging
- Message passing
- Interrupts and MSI

THE PCI EXPRESS INTERFACES

- 8-lane host interface
- 4-lane secondary interfaces
- Root complex vs EndPoint configuration
- PCI Express functional cores
- Hardware implementation
- Power management
- Error handling
- Messaging

THE FAST ETHERNET CONTROLLER

- 802.3 specification fundamentals : PHY and MAC layers
- 440SPE Ethernet controller organization
- PHY
- Flow control
- VLAN support
- Frame filtering
- Hash table usage in switch applications
- Memory Access Layer controller, buffer management
- Buffer descriptors initialization
- Errors management

THE XOR ACCELERATOR UNIT

- Parity generation and check functions
- Command block list
- DMA capability

THE I2O MESSAGE UNIT / DMA CONTROLLER

- Message vs doorbell
- Management of inbound messages
- Management of outbound messages
- DMA operation

STANDARD PERIPHERALS

- GPIO
  - GPIO interface signals
  - Pin configuration
- UART
  - FIFO mode
  - Flow control signals management
- IIC
  - IIC protocol fundamentals
  - Transmission and reception sequence
  - Serial boot ROM

Renseignements pratiques

Duration : 5 days
Cost : 2100 € HT