PC1 - PPC750CXe/FX/FM/GX/GL implementation

This course covers the IBM Power 750CXe, 750FX, 750FM, 750GX and 750GL Power G3 CPUs

Objectives

- A focus is done on the PowerPC EABI which is fundamental when C programs are to be interfaced with assembly routines.
- The pipeline is viewed in detail in order to infer instructions scheduling guidelines.
- Many Diab Data PowerPC specific compiler options are studied.
- A flush routine is used to explain data flows between L1 data cache, L2 cache and SDRAM main memory.
- The course details the segmentation / pagination mechanism used to protect process.
- A generic exception handler is described.
- The hardware implementation is also covered.
- The course emphasizes differences between 750CXe, 750FX and 750GX.

- This training has been delivered several times to companies developing avionics and defence equipments.
- ACSYS also offers trainings on Marvell Discovery host bridges that can be used as companion chips for IBM G3 CPUs.

Labs are compiled with Diab Data compiler and run under Lauterbach Trace32 debugger.
A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

THE INSTRUCTION PIPELINE

- 750 implementation : superscalar operation, out-of-order execution, register renaming, serializations, isync instruction
- Branch processing unit : BTIC, guarded memory
- Branch instructions
- Coding guidelines

DATA PATHS

- Load / store architecture
- Data path between L1 and L2
- Load / store buffers
- Sync and eieio instructions
- Store gathering mechanism

CACHES

- Cache basics
- L1 caches : PLRU algorithm
- Miss under miss operation
- Shared resource management
- Cache coherency mechanism, snooping, related signals
- The MEI state machine
- Management of cache enabled pages shared with PCI DMAs
- Reservation coherency
- Cache related instructions
- Cache flush routine
- The L2 cache, organization, replacement algorithm
- L2 cache locking by way (750FX/FL, 750GX/GL)

SOFTWARE IMPLEMENTATION

- PowerPC architecture specification, the 3 books UISA, VEA and OEA
- Addressing modes
- Integer instructions
- IEEE754 basics, floating points numbers encoding
- Floating point arithmetical instructions
- Improvements implemented in the 750FX/FL/GX/GL : additional reservation station and quicker reciprocal estimates
- The PowerPC EABI
- Linking an application with Diab Data

THE MMU

- Thread vs process
- Introduction to real, block and segmentation / pagination translations
- Memory attributes and access rights definition
- Virtual space benefit, page protection through segmentation
- TLBs organization
- Segmentation : process ID definition
- Pagination : PTE table organization
- Explanation of hash value and API field
- MMU implementation in real-time sensitive applications

THE EXCEPTION MECHANISM

- Save / restore registers SRR0/SRR1, rfi instruction

- Exception management mechanism
- Requirements to allow exception nesting
- PowerPC timers TB and DEC

HARDWARE IMPLEMENTATION

- Hreset vs Sreset
- Clocking
- Bus operation
- Address phase
- Data phase
- Address decode logic design
- Timing analysis
- Minimal implementation
- Low power modes
- Power, dual PLLs for seamless frequency switching (750FX/FL, 750GX/GL)

THE PERFORMANCE MONITOR

- Objectives of the performance monitor
- Event counting
- Programming interface

THE DEBUG PORT

- JTAG emulation
- Real time trace requirements
- Code instrumentation
- Hardware breakpoints

Renseignements pratiques

Duration : 5 days
Cost : 2100 € HT