IP2 - USB 2.0

This course covers USB2.0

Objectives

- The course details the hardware implementation and describes the tests required to check the compliance of an equipment.
- All interconnect standards between Link and PHY are explained: UTMI, UTMI+, ULPI as well Inter-Chip USB.
- An architectural view of an USB system implementing low speed, full speed and high speed devices is described.
- The course details the various steps of the bus enumeration sequence.
- Packet format and USB transactions are taught with the assistance of the Lecroy USB analyser.
- The course details the requirements of the EHCI specification.
- HID class device specification and mass-storage classes are covered on request.

A Lecroy USB analyser is used to capture and display USB traffic.

• A lot of traces are included in the material.

A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites

- Experience of a digital bus is mandatory.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

SYSTEM ARCHITECTURE

- Introduction to USB
- Management of periodic traffics
- Software organization
- Highlighting the differences between transfer, transaction and packet
- Device configuration, standard descriptors and commands

ELECTRICAL SPECIFICATION

- Cable and connectors
- Low Speed / Full Speed signalling
- Reset sequence
- High Speed signalling
- Reset sequence, chirp negotiation

TRANSFER PROTOCOL

- Low Speed / Full Speed protocol
- Periodic traffics in High Speed systems
- Non periodic traffics in High Speed systems
- Error detection
- Power management

BUS CONFIGURATION

- Device configuration Standard descriptors
- Device configuration Standard commands
- Initialization sequence
  - A trace is studied to understand the initialization sequence by using the ability of the trace viewer to decode standard requests
- Purpose of USB classes, list of classes

USB ON-THE-GO 2.0

- Typical applications
- New plug and receptacles
- Electrical requirements
- Attach Detection Protocol
- Session Request Protocol
- Host Negociation Protocol
- Testing the interface

BATTERY CHARGING SPECIFICATION

- Accessory Charger Adapter
- Charger detection hardware
- Primary detection
- Secondary detection
- Charger detection algorithms
- Electrical requirements

HUB OPERATION

- Hub architecture
- Split transactions

- The Hub class - Descriptors
- The Hub class - Commands
  - A trace is studied to understand the configuration of a hub by using the ability of the trace viewer to decode hub class requests

TRANSCEIVER STANDARD INTERFACES

- UTMI, elastic buffer, transmit and receive transmit diagrams
- Carkit, multiplexing USB traffic, UART and analog audio on the USB cable
- UTMI+ 1.0, description of new signals required to support OTG
- UTMI+ 1.0, level 2 and 3
- ULPI 1.1, low pin count interface, transfer protocol

HOST CONTROLLER OPERATION

- OHCI
- UHCI
- Introduction to EHCI
- Host Controller initialisation
- Port routing and control
- Periodic schedule
- Asynchronous schedule
- Managing Control / Bulk / Interrupt transfer via Queue Heads

DEBUGGING A USB APPLICATION

- Compliance checklists released by the USB Implementers Forum
- USB2.0 electrical test specification
- Detailing the list of tests to be run on the oscilloscope
- Lecroy solutions: protocol analysers / exercicers, test of the physical layer

HID CLASS DEVICES [On request]

- Operational model, item parser, report ID
- Descriptors, HID descriptor, report descriptor: main item, global item, local item
- Requests: GetReport/SetReport, GetIdle/SetIdle, GetProtocol/SetProtocol
- Boot interface descriptors: mouse and keyboard
  - A trace related to a mouse is used all along this chapter to provide practical examples of HID report descriptor and mouse report transfer format

MASS STORAGE CLASS DEVICES [On request]

- Relationship with ATAPI specification
- Reduced Block commands
- SCSI primary commands
- MMC command set
- Control, Bulk, Interrupt transport
- Standard descriptors
- Bulk only transport
  - USB memory stick traffic has been captured to explain the various protocols described in this chapter

USB FOR SMARTCARD [On request]

- Basics of ISO/IEC 7816-3
- Answer To Reset
- Protocol and Parameter Selection
- Interchip USB, voltage class negotiation
- Interchip USB, device attachment / detachment, highlighting when RPU and RPD have to be connected and disconnected
- ETSI TS 102 600 UICC-Terminal interface, Characteristics of the USB interface
- SimCard, ICCD class, transporting ISO messages over USB
- Managing a POS, CCID class

AUDIO CLASS [On Request]

- Audio device types
- Synchronization issues, difference between synchronous and isochronous
- Synchronous, asynchronous and adaptive synchronizations
- Feedback pipe
- Isochronous endpoint descriptor
- Interface descriptor
- Audio Control
- Unit descriptors
- Audio specific requests
- Retrieving the audio system architecture through the chained units and terminals

Renseignements pratiques

Duration : 4 days
Cost : 2490 € HT