II1 - DigRF and RFFE

This course covers DigRF and RFFE MIPI buses

Objectives

- The course starts with an overview of MIPI specification.
- Chapters are studied with a bottom-top approach, starting with M-PHY and ending with RFFE.
- DigRF protocol, particularly frame acknowledgment, is detailed.
- The course describes the DigRF startup sequence.
- Connection to the antenna via RFFE is explained, focusing on both physical layer and protocol.
- Test modes are also covered.
- Companies interested in attending this course must adhere to MIPI organization.
- This course has been designed for engineers in charge of SoC architecture, functional verification or silicon validation.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Basic knowledge on digital electronics.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION TO MIPI SPECIFICATIONS

M-PHY

- Termination scheme
- Signaling schemes
- M-PHY type II modules
- Embedding clock into the bitstream, 8b10b coding
- DC-balancing, running disparity
- PHY state definition
- HS-MODE BURST Operation
- SYS-BURST operation
- Configuration attributes
- Test modes
- Electrical characteristics, eye-diagrams
- Jitter influence on LINE characterization
- Recommended test functionality

DIGRF INTERFACE

- Overview
- Physical layer based on M-PHY Type-II
- 8b/10b control character mapping
- Interface states
- Protocol
- Programming model

DEVICE DESCRIPTOR BLOCK (DDB)

- Services to transfer descriptor and configuration data between devices on a MIPI Interconnect
- Underlying interconnect requirements
- DDB-PDU format
- DDB protocol support for Level 1 and Level 2 services

RF FRONT-END CONTROL INTERFACE (RFFE)

- Two-wire, serial interface
- Point-to-multipoint connectivity
- Time-accurate triggering mechanisms
- MIMO configuration
- Operating states
- Physical layer
- Protocol layer
- Command sequences
- Broadcast messages
- Device enumeration, device identification

Renseignements pratiques

Duration : 2 days
Cost : 1350 € HT