IC5 - RapidIO 3.0

This course covers the RapidIO interconnect version 3.0

Objectives

- Packet switching benefits compared to shared busses are highlighted.
- The course explains the various traffic types that RapidIO supports: Input / output, Message and GSM.
- Mechanisms like error recovery and flow control are explained through various sequences.
- The course covers all features present in the RapidIO 3.0 specification, such as end-to-end flow control, multicast programming, data streaming and virtual output queuing extensions.
- CC-NUMA cache coherency mechanism is studied.
- The course describes the discovery sequence required to initialize the switches.
- Details of RapidIO interfaces present in NXP and IDT devices are provided to explain how theoretical statements are actually implemented .

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a digital bus such as PCI or Ethernet.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

THE TRANSITION TO PACKET SWITCHING

- Limitations of parallel shared buses
- Benefits of differential transmission
- Gigabit Serdes

INTRODUCTION TO RAPIDIO

- Layer model, features of logical, transport and physical layers
- Packet encapsulation
- Purpose of control symbols
- Technical features: distributed memory vs message passing

THE INPUT / OUTPUT LOGICAL TRAFFIC

- Accessing memory mapped address ranges
- Accessing the configuration space
- Atomic transactions
- Maintenance transaction
- Port write operation

THE MESSAGE PASSING LOGICAL TRAFFIC

- Message vs doorbell
- Transmission of interrupts through doorbells, concept of virtual wires
- Management of messages split into several packets
- Detail of message passing implementation in NXP QorIQ devices

CACHE COHERENCE

- Snooping basics
- GSM transactions, coherence domains
- The CC-NUMA approach
- Description of a directory entry: the sharing mask
- Analysis of various cache coherency sequences

DATA STREAMING LOGICAL SPECIFICATION

- Mechanism of transporting an arbitrary protocol over a standard RAPIDIO interface
- Traffic streams
- Encapsulation methodology
- Support for PDU of 64 kB through segmentation and reassembly
- Class of services and virtual queues

LOGICAL LAYER FLOW CONTROL

- Controlled flow list
- Watermarks setting
- XON-XOFF controls on transaction request flows
- Physical layer requirements
- Ordering rules

THE TRANSPORT LAYER

- Packet routing through the network based on destination ID
- Programming interface to read / write the routing tables

- Multicast extensions
- Multicast mask and multicast group

SYSTEM BRINGUP

- System exploration and initialization
- System enumeration API
- Hardware abstraction layer

OVERVIEW OF THE PHYSICAL LAYER

- Packet acknowledgement
- Control symbols vs packet
- Multicast event

ERROR MANAGEMENT

- Early processing of packets
- Study of various sequences explaining the ability of RAPIDIO to recover from errors automatically by hardware
- Port behaviour when error rate failed threshold is reached
- Drop packet enable
- Hot Swap Extensions
- Port behaviour when error rate failed threshold is reached
- Drop packet enable
- System software notification of errors

PACKET PRIORITY AND FLOW CONTROL

- Mapping flowID into 2-bit priority
- Receiver based flow control, retry mechanism
- Transmitter based flow control, management of transmit credits
- Deadlock prevention

THE LP-LVDS 8/16 INTERFACE (On request)

THE LP-S 1x/4x INTERFACE

- Features or sublayers PCS and PMA
- Format of packets and symbols
- Single VC mode vs multiple VC mode, purpose of VC status control symbol
- The 8b/10b encoder / decoder
- Special characters, comma detection
- Lane synchronization
- 1.25Gbaud, 2.5Gbaud, and 3.125Gbaud LP-Serial Links
- 5Gbaud and 6.25Gbaud LP-Serial Links
- Transmit emphasis tuning
- Use of eye diagram to specify the electrical interface

THE LP-S 1x/4x INTERFACE 10.3125 Gbaud OPERATION

- 64B/67B PCS and PMA Layers
- Scrambling
- Ordered sequences
- Electrical Specification for 10.3125 Gbaud LP-Serial Links
- Adaptive Equalization

VIRTUAL OUTPUT QUEING EXTENSIONS

- Head Of Line blocking
- Congestion message

- Traffic staging
- Relationship with VC

Renseignements pratiques

Duration : 3 days
Cost : 2000 € HT