# IC1 - PCI 3.0

## This course covers PCI bus version 3.0

## Objectives

- The training has been designed from the PCI3.0 specification.
- It describes the read prefetch / write posting mechanisms and synchronization rules.
- Transfer protocol is explained with the assistance of the Lecroy analyzer board.
- The course emphasizes the host bridge operation especially the management of PCI accesses targetting cache enabled regions.
- A software routine has been developped to show how to access the configuration space.
- Also interrupt requests allocation, memory regions allocation are detailed in single PCI system and multiple PCI systems (PCI-to-PCI bridge).
- The course explains how to tune the PCI performance: selecting optimized LT value, appropriate master priority, enabling fast-back-to-back.

*A more detailed course description is available on request at formation@ac6-formation.com*

### Prerequisites

- Experience of a digital bus is mandatory
- Experience of a 32-bit processor is recommended

### Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

### Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

### Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

# Plan

## OVERVIEW

- PCI specifications history
- PCI bus features
- PCI device types
- Technological introduction
- Architecture of recent PCs

## PCI DEVICE ARCHITECTURE

- Information buffering
- Buffer management
- Prefetchable vs non-prefetchable memory ranges
- Synchronization rules
- Producer / consumer model
- Optional processings
- PCI bus limitations

## TRANSFER PROTOCOL

- Transfer basics
- Pinout, signal classes
- Arbitration
- Data transfer protocol
- Address decoding in IO, MEM and CFG spaces
- 64-bit data transfer
- 64-bit addressing
- Master initiated terminations
- Target initiated terminations
- Fast back-to-back
- Parity control
- Shared resource management
- Bus analyse, benefit of a bus analyser / exerciser

## INTERRUPTS AND RESET

- PCI interrupts
- Interrupt acknowledge transaction
- Interrupt sharing
- Message Signaled Interrupts
- MSI-X
- Reset, operating states

## CACHE COHERENCY

- Cache basics
- Snooping basics
- Cacheability of RAM accessed by the host CPU through PCI
- PCI masters accessing the host memory
- PCI agent processor accessing the host memory

## ELECTRICAL SPECIFICATION

- Switched wave switching vs Incident wave switching
- Static specification
- Dynamic specification : 33 MHz and 66 MHz

- Clocking
- Decoupling
- Routing and layout recommendations
- Compliance checklists

## CONFIGURATION SPACE

- Configuration space mappings
- Register description
- PCI MEM and PCI IO mappings building
- Expansion ROM
- Capability list
- Configuration transactions, IDSEL routing
- Local vs distant CFG transaction
- Generation of config transactions

## PCI-TO-PCI TRANSPARENT BRIDGES

- Bus numbering
- Address decode, transaction forwarding rules
- Distant configuration cycles
- Error management

## POWER MANAGEMENT

- Bus power state machine
- PCI function power state machine
- Programming interface

## PCI BASED INDUSTRIAL SPECIFICATIONS

- Passive bus PICMG PC
- CMC/PMC mezzanine boards, BUSMODE pins management
- CompactPCI introduction
- PC104+ introduction
- PC.MIP introduction

## Renseignements pratiques

**Duration : 3 days**
**Cost : 2130 € HT**