FM5 - MPC5674F implementation

This course covers NXP Qorivva MPC5673F and MPC5674F

Objectives

- This course has 6 main objectives:
  - Detailing the hardware implementation of the MPC56XX
  - Parameterizing the internal interconnect and sophisticated eDMA controllers
  - Focusing on the various operation modes supported by the eQADC
  - Describing the timer units, including eTPU2
  - Describing the communication interfaces, including FlexCAN and FlexRay
  - Studying the debug capabilities offered by the Nexus interface.
- Products and services offered by AC6:
  - AC6 is able to assist the customer by providing consultancies
  - Typical expertises are done during board bringup, hardware schematics review, software debugging, performance tuning.

They have been developed with Diab Data compiler and are executed with TRACE32 Lauterbach debugger.

A more detailed course description is available on request at formation@ac6-formation.com
This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Prerequisites and related courses

- Experience of a 32-bit processor or DSP is mandatory.
- Note that the e200z7 Power core is covered in a separate course reference FCC3 - e200z7 implementationcourse.
- The following courses could be of interest:
  - FlexRay, reference IA2 - FlexRay 2.1course
  - CAN bus, reference IA1 - CAN buscourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented

- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

MPC5674F ARCHITECTURE

OVERVIEW

- Compatibility with MPC55XX family
- Memory mapping
- e200z7 core integration

HARDWARE IMPLEMENTATION

POWER, RESET AND CLOCKING

- Power management controller
- Reset
- Clocking
- Boot assist module (BAM)

SYSTEM INTEGRATION UNIT

- Pad configuration control for each pad
- System reset monitoring and generation
- External interrupt pins
- General Purpose Input Output setting
- Internal peripheral multiplexing

EXTERNAL BUS INTERFACE

- Multiplexed address/data transfers
- Chip-select programming
- Burst support
- Dynamic calibration with up to 4 chip-selects

ANALOG-TO-DIGITAL CONVERTERS (eQADC)

- 64 analog channels, differential conversions
- ADC clock and conversion speed
- ADC calibration feature
- MAC unit and operand data format
- Variable gain amplification
- CFIFO0 streaming mode
- 8 decimation filters
- Temperature sensor
- Time stamp information
- Trigger sources
- External multiplexing
- Interrupt or DMA request generation

SOC PLATFORM

INTERNAL INTERCONNECT

- Crossbar switch
- Peripheral Bridge
- Memory Protection Unit

ERROR CORRECTION STATUS MODULE

- Status information regarding platform memory errors

INTEGRATED MEMORIES

- 256-KB on-chip SRAM
- 4-MB on-chip flash

INTERRUPT CONTROLLER

- Priority-based preemptive scheduling
- Preemptive prioritized interrupt requests to processor
- Software-configurable priorities of ISR or tasks
- Software vector mode vs hardware vector mode

ENHANCED DIRECT MEMORY ACCESS CONTROLLER (eDMA)

- DMA request assignments
- Transfer control descriptors
- Channel-to-channel linking mechanism
- Peripheral-paced hardware requests
- Channel arbitration
- Scatter/gather DMA processing
- Modulo feature

CONNECTIVITY

ENHANCED SERIAL COMMUNICATION INTERFACES(eSCI)

- Introduction to LIN specification
- Idle line detection
- LIN master node functionality
- Detection of bit errors, physical bus errors and checksum errors
- DMA support for both transmit and receive data

FLEXCAN MODULE

- Hardware interface
- 64 message buffers of zero to eight bytes data length
- Individual Rx mask registers per message buffer
- Powerful Rx FIFO ID filtering
- Management of remote frames, overload frames
- Listen-only mode capability
- Time stamp based on 16-bit free-running timer

DESERIAL SERIAL PERIPHERAL INTERFACE (DSPI)

- Serial Peripheral Interface (SPI) configuration

- Deserial Serial Interface (DSI) configuration
- Combining Serial Interface (CSI) configuration
- Enhanced Deserial Serial Interface (DSI) configuration
- Queued operation

DUAL-CHANNEL FLEXRAY CONTROLLER

- Hardware interface
- FlexRay memory layout
- Message buffer concept
- Buffer locking scheme
- Message buffer states
- Individual message buffer reconfiguration supported
- Filtering on FrameID, ChannelID, MessageID
- Slot error counters

TIMERS

SYSTEM TIMERS

- System Timer Module
- Periodic Interrupt Timer, Real Timer Interrupt
- SWT

ENHANCED MODULAR INPUT OUTPUT SYSTEM (EMIOS200)

- Shared time bases with the eTPU
- Output Pulse Width Modulation (OPWM) mode
- Input Pulse-Width Measurement (IPWM) mode
- Pulse/Edge Accumulation (PEA) mode
- Quadrature decode (QDEC) mode
- Windowed Programmable Time Accumulation (WPTA) mode
- Output Pulse Width and Frequency Modulation (OPWFM) mode
- Pulse-Width and Frequency Modulation Buffered (OPWFMB) mode
- Center Aligned Output Pulse Width Modulation with Dead Time (OPWMC) mode
- Center-Aligned Output PWM Buffered with Dead Time (OPWMCB) mode

eTPU2

- Hardware interface
- Time base
- Event-triggered microengine
- Functions and threads
- Host interface
- Scheduling channel service requests
- Parameter sharing and coherency
- Implementing functions developed by NXP

GLOBAL FUNCTIONS, DEVELOPMENT AND DEBUG

NEXUS DEBUG UNIT

- Introduction to NEXUS specification
- Data trace via data write messaging and data read messaging
- Ownership trace via ownership trace messaging
- Program trace via branch trace messaging
- Watchpoint messaging via the auxiliary port
- Run-time access to the on-chip memory

Renseignements pratiques

Duration : **4 days**
Cost : **1950 € HT**