FM3 - eTPU programming

This course covers eTPU code generation and simulation

Objectives

- The course explains the CPU-like TPU architecture.
- CPU-to-TPU interface is detailed.
- The course highligths all channel operation modes.
- The course focuses on various fields of the instructions enabling concurrency.
- The scheduler priority algorithm is detailed in order to estimate the worst case latency for channel service.
- Micro-coding and debugging an application composed of several states is explained through practical examples.

- This course has been delivered several times to companies developing automotive systems.

A lot of programming examples have been developed by ACSYS to explain the eTPU operation.
- *They have been developed with Ashware tools.*

A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites

- Basic knowledge about microprocessor architecture, hardware timer and assembler instructions and directives.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION TO TPU

- Locating the TPU in different components proposed by NXP
- Objectives of a such approach
- Quick presentation of standard functions

TPU ARCHITECTURE

- The various modules and interactions between them
- Micro-engine
- Ram
- Host interface
- Rom
- Channel
- Scheduler

CHANNEL DESCRIPTION

- Features
- Block diagram
- State at Reset
- Configuring a channel
- Transition event
- Match event
- Full default modes study
- Channel link

RAM PARAMETER

- Mapping
- The addressing modes
- Timing
- Coherency

SCHEDULER ARCHITECTURE

- Sources of service requests
- Requests hierarchy
- Preemptivity
- State selection

TPU MICROCODE OVERVIEW

- VLIW machine
- Instruction format

MICRO-ENGINE PROGRAMMING MODEL

- Registers list
- Execution unit hardware
- Code condition latch
- Channel selection
- Loop
- Arithmetic instructions
- Multiply and Mac instructions

FLOW CONTROL INSTRUCTIONS

- Pipeline
- Branch chart
- Conditional branches
- Flush pipe or not
- Repeat capabilities
- Call and return instructions

THE ENTRY POINTS

- Entry table chart
- Scheduler behavior, inner channel priority management
- Entry directive
- Entry points general format

THE SCHEDULER OPERATION

- Sources of service request
- Service requests priority
- Selected state address generation
- Priority scheme

CHANNEL SERVICE WORST CASE LATENCY

- Threads switch timing
- Taking into consideration other requests
- Access concurrency delay

IMPLEMENTATION

- This part may be tailored to customers needs during on-site trainings.
- For instance developing a UART function with parity generation / checking can be used to understand all the previous topics.

Renseignements pratiques

Duration : 3 days
Cost : 1650 € HT