FA4 - i.MX6 Implementation

This course describes the i.MX6 Dual and Quad core SoC

OBJECTIVES

- The course details the hardware implementation of the i.MX6 SoC.
- The course focuses on the boot sequence, the clocking and the power management strategies.
- The course explains all parameters that affect the performance of the system in order to easily perform the final tuning.
- The multiple complex units involved in multimedia management are covered in depth.
- An overview of the Cortex-A9MP core helps to understand issues caused by MMU, cache and snooping.
- Interrupt management through ARM GIC is explained through a lab.
- The course also covers the hardware implementation, particularly the DDR3 and NAND flash controllers.

- Note that these course outlines cover all units within the i.MX6
  - According to the actual reference chosen by the customer, some chapters may be removed.

- Products and services offered by ACSYS:
  - ACSYS is able to assist the customer by providing consultancies. Typical expertises are done during board bringup, hardware schematics review, software debugging, performance tuning.

This course is only provided on-demand; A more detailed course description is available on request at formation@ac6-formation.com
This document is necessary to tailor the course to the specific customer needs and to define the exact schedule.

Prerequisites and related courses

- This course provides only an overview of the Cortex-A9MP
- Our course reference R1 - ARM7/9 implementationcourse details the operation of this complex ARM CPU.
- Our course reference RC1 - NEON-v7 programmingcourse explains how to vectorize and implement algorithms to be executed by NEON SIMD engine.

- The following courses could be of interest:
  - USB Full Speed High Speed and USB On-The-Go, reference IP2 - USB 2.0course
  - Ethernet and switching, reference N1 - Ethernet and switchingcourse
  - IEEE1588, reference N2 - IEEE1588 - Precise Time Protocolcourse
  - CAN bus, reference IA1 - CAN buscourse
  - Memory cards, reference IS2 - eMMC 5.0course
  - SATA, reference IS3 - Serial ATA IIIcourse
  - PCI Express, reference IC4 - PCI Express 3.0course

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

ARCHITECTURE OF i.MX6

- ARM core based architecture
- On-chip memories
- Clarifying the internal data paths: AXI interconnect, AHB bus, peripheral buses
- Organization of a board based on i.MX6
- Memory mapping

SYSTEM CONTROL

- IOMUX module, understanding how to select the function supported by each pin
- Pad settings
- General Purpose Input interrupt request capability

THE ARM CORTEX-A9MP CORE - OVERVIEW

- Instruction sets
- Pipeline description
- MMU and TLBs
- Level 1 caches
- Cache coherency

THE CORTEX-A9MP PLATFORM

- Cortex-A9MP and PL310 L2 cache IP instantiation options
- Integrated interrupt controller (GIC), detail of interrupt mapping
- AHB to IP Bridge
- AHB-to-APBH Bridge with DMA
- NIC-301 AXI interconnect

RESET AND CLOCKING

- Power supplies
- Clock Control Module
- System Reset Controller
- General Power Controller

DEBUG ARCHITECTURE

- Introduction to CoreSight, DAP features
- System Secure Controller SJC
- Embedded Trace Macrocell

- Cross Triggering Interfaces

SYSTEM SECURITY

- ARM TrustZone architecture
- Cryptographic Acceleration and Assurance Module
- Secure Non Volatile Storage
- Run-Time Integrity Checker
- Central Security Unit
- Advanced High Assurance boot

SMART DMA CONTROLLER

- Overview, basic script routines
- Mapping DMA requests to channels
- Channel priority definition
- Scheduler
- Instruction description
- PCU states
- Context switching

ACCESSING EXTERNAL MEMORIES

- Multi-Mode DDR Controller
- General-Purpose Media Interface
- EIM unit

MASS-STORAGE INTERFACES

- S-ATA II
- Ultra SDHC

VIDEO PROCESSING UNITS

- A simple processing flow of Multimedia application
- Video Processing Unit
- Image Processing Unit v3
- Graphics Processing Unit 2D
- Graphics Processing Unit 3D

AUDIO RELATED INTERFACES

- Overview of audio subsystem
- SSI interfaces
- Digital audio multiplexor
- SPDIF transmitter
- Enhanced Serial Audio Interface (ESAI)
- Asynchronous Sample Rate Converter
- PWM

PCIe CONTROLLER

- Gen 2 operation
- 1-lane
- Configuration as Agent or Root Complex
- Interrupt management
- PHY parameterizing

COMMUNICATION CONTROLLERS

- HSI

- Enhanced CSPI
- I2C interfaces
- UART
- USB
- Gigabit Ethernet Controller
- MediaLB
- FlexCAN controllers

Renseignements pratiques

Duration : 5 days
Cost : 2790 € HT