



## ARM Cores

### Courses on ARM cores

ACSYS offers a large set of courses on ARM processor cores.

Each course details both hardware and software implementation of these cores.

Programming examples are provided to clarify the operation of complex assembly instructions and to explain the parameterizing of the ARM linker. **AAA - ARM Cortex-A and R Architecture** This course explains the ARM Cortex-A and R global architecture. It provides the prerequisites needed to start learning the various ARMv7 A&R specific cores. It also briefly outlines the ARMv8 64bit architecture.

**AAM - ARM Cortex-M Architecture** This course explains the ARM Cortex-M global architecture. It provides the global understanding of the ARMv7 and v8 Cortex-M architecture needed to efficiently program MCU based on such cores.

**RA0 - Cortex-A5 implementation** This course covers the ARM Cortex-A5 CPU

**RA1 - Cortex-A8 implementation** This course covers the Cortex-A8 high-end ARM core

**RA2 - Cortex-A9 implementation** This course covers both Cortex-A9 single and multiple core high-end ARM CPUs

**RA3 - Cortex-A15 implementation** This course covers Cortex-A15 high-end ARM CPU

**RA4 - Cortex-A7 implementation** This course covers Cortex-A7 ARM CPU

**RA5 - Cortex-A17 implementation** This course covers the Cortex-A17 cluster

**RA6 - CORTEX-A57 implementation, ARM Architecture V8** This course covers the Cortex-A57 and AARCH64

**RA7 - CORTEX-A53 implementation, ARM Architecture V8** This course covers the Cortex-A53 and AARCH64

**RA8 - CORTEX-A72 implementation, ARM Architecture V8** This course covers the Cortex-A72 and AARCH64

**RA9 - CORTEX-A73 implementation, ARM Architecture V8** This course covers the Cortex-A73 and AARCH64

**RC1 - NEON-v7 programming** This course explains how to use ARMv7 NEON SIMD instructions to boost multimedia algorithms

**RC2 - NEON-v8 programming** This course explains how to use ARMv8 NEON SIMD instructions to boost multimedia algorithms

**RI0 - AXI3 / AXI4 INTERCONNECT** This course covers the AXI bus protocol, described in ARM AMBA v3 and v4

**RM0 - Cortex-M0 / Cortex-M0+ implementation** This course covers both Cortex-M0 and Cortex-M0+ ARM CPUs

**RM1 - Cortex-M1 implementation** This course covers the Cortex-M1 ARM core targeting FPGA SoCs

**RM2 - Cortex-M3 implementation** This course covers the Cortex-M3 ARM core

**RM3 - Cortex-M4 / Cortex-M4F implementation** This course covers both Cortex-M4 and Cortex-M4F (with FPU) ARM core

**RM4 - Cortex-M7 implementation** This course covers the Cortex-M7 V7E-M compliant CPU

**RM5 - Cortex-M33 Implementation** This course covers the Cortex-M33 ARMv8 core

**RR0 - Cortex-R4 implementation** This course covers the Cortex-R4 ARM core

**RR1 - Cortex-R5 implementation** This course covers the Cortex-R5 / Cortex-R5F ARM cores

**RR2 - Cortex-R7 implementation** This course covers the Cortex-R7MP ARM cores