



This course covers PowerQUICC III devices, including MPC8560

Objectives

- The course details the internal data path, particularly the Ocean crossbar that interconnects e500, RapidIO, DDR SDRAM, PCI and external bus.
- Cache coherency protocol is introduced in increasing depth.
- The course describes both hardware and software implementation of gigabit Ethernet controllers.
- The MCC superchanneling is examined.
- The ATM traffic shaper is viewed in detail.
- A long introduction to DDR SDRAM operation is done before studying the DDR SDRAM controller.
- An in-depth description of the RapidIO port and the PCI-X port is performed.

- This course has been delivered several times to companies developing telecom infrastructure equipments.

- ACSYS has developed an optimized SPE based FFT coded in assembler language.
- Performance for 1024 complex floating point single precision samples is:
 - - 91_386 core clock cycles without reverse ordering, 94_124 with reverse ordering
- Performance for 4096 complex floating point single precision samples is:
 - - 470_778 core clock cycles without reverse ordering, 511_227 with reverse ordering
 - for any information contact formation@ac6-formation.com

A lot of programming examples have been developed by ACSYS to explain the boot sequence and the operation of complex peripherals, such as Gigabit Ethernet.

• They have been developed with Diab Data compiler and are executed with Lauterbach Trace32 debugger.

A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites and related courses

- Experience of a 32 bit processor or DSP is mandatory.
- The knowledge of the following interconnect standards may be required:
 - RapidIO see our course reference cours [IC5 - RapidIO 3.0](#)
 - PCI-X, see our course reference cours [IC3 - PCI-X 2.0](#)
 - Gigabit Ethernet, see our course reference cours [N1 - Ethernet and switching](#)

Environnement du cours

- Cours théorique
 - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
 - Cours dispensé via le système de visioconférence Teams (si à distance)
 - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Modalités d'évaluation

- Les prérequis indiqués ci-dessus sont évalués avant la formation par l'encadrement technique du stagiaire dans son entreprise, ou par le stagiaire lui-même dans le cas exceptionnel d'un stagiaire individuel.
- Les progrès des stagiaires sont évalués par des quizz proposés en fin des sections pour vérifier que les stagiaires ont assimilé les points présentés
- En fin de formation, une attestation et un certificat attestant que le stagiaire a suivi le cours avec succès.
 - En cas de problème dû à un manque de prérequis de la part du stagiaire, constaté lors de la formation, une formation différente ou complémentaire lui est proposée, en général pour conforter ses prérequis, en accord avec son responsable en entreprise le cas échéant.

Plan

INTRODUCTION TO THE MPC8560

- Internal data path, OCEAN switch fabric, packet reordering
- Address map, ATMU
- Local vs external address spaces, inbound and outbound address decoding
- Accessing CCSR memory from external master

THE e500 CORE

- The instruction pipeline
- Dynamic branch prediction
- The first level MMU and the second level MMU
- Process protection
- The L1 caches
- Level 2 cache
- e500 coherency module
- Load store unit, data buffering between LSU and CCB
- Signal Processing APU (SPU)
- PowerPC EABI
- Book E exception handling
- Power management
- JTAG emulation

RESET, CLOCKING AND INITIALIZATION

- Platform clock
- Power-on reset sequence, use of the I2C interface to access serial ROM
- Boot page translation

THE DDR-SDRAM CONTROLLER

- DDR-SDRAM operation : a 128-Mbits DDR-SDRAM from Micron is used as an example
- Jedec specification basics, mode register initialization, bank selection and precharge
- Command truth table
- Bank activation, read, write and precharge timing diagrams, page mode
- DDR-SDRAM controller introduction
- Initial configuration following Power-on-Reset
- Address decode
- Timing parameters programming
- Initialization routine

LOCAL BUS CONTROLLER

- Multiplexed 32-bit address and data transfers
- Burst support

- Dynamic bus sizing
- GPCM, UPMs and SDR SDRAM states machines

RapidIO INTERFACE UNIT

- 8-pin parallel interface, LVDS signalling
- Packet pacing support at the physical layer
- Atomic operations
- RapidIO compliant message unit

PCI/PCI-X FUNCTIONAL UNITS

- Data flows : Read prefetch and write posting FIFOs
- Inbound transactions handling, outbound transactions handling in both modes
- Support of multiple split transactions in PCI-X mode
- PCI-to-memory and memory-to-PCI streaming

LOW SPEED PERIPHERALS

- Programmable Interrupt Controller
- Interrupt nesting
- Description of the 4 timers / counters
- Message interrupts
- I2C controller

THE THREE-SPEED ETHERNET CONTROLLERS TSECs

- Physical interfaces : GMII, MII, TBI or RGMII
- Buffer descriptor management
- Layer 2 acceleration accept or reject on address or pattern match
- 256-entry hash table for unicast and multicast
- Direct queuing of four flows

INTEGRATED DMA CONTROLLER

- Priority between the 4 channels
- Scatter / gathering
- Selectable hardware enforced coherency

INTRODUCTION TO CPM

- CP operation : peripheral prioritization
- Command register
- DPRAM organization
- IDMA vs SDMA

THE SERIAL INTERFACE

- NMSI versus TDM
- MCC connection to SI
- Baud rate generators
- Communication initialization sequence
- Buffer descriptor ring allocation in DPRAM
- Buffer chaining

THE MULTI CHANNEL CONTROLLERS

- DPRAM organization
- Time slot vs logic channel
- Super channels
- HDLC channel parameters

- Interrupt queues

THE SERIAL COMMUNICATION CONTROLLERS

- Data encoding /decoding selection
- Hardware flow management
- HDLC on SCC
- Ethernet on SCC : address recognition, hash table programming

FAST ETHERNET CONTROLLER

- 802.3u basics
- MII interface
- Hash tables utility
- Parameter RAM description

ATM BASICS

- ATM benefit compared to X.25 or ISDN
- UNI and NNI network interfaces
- Cell format
- Virtual connection
- Layer model
- AAL1 layer : circuit emulation
- AAL3/4 : used by the service providers
- AAL5 : packet transfer
- Connection establishment

ATM TRAFFIC MANAGEMENT

- The 5 service classes defined by the ATM forum : CBR, VBRrt, VBRnrt, UBR, ABR
- The QoS ATM attributes : PCR/CDVT, CLR, CTD/CDV
- Traffic policy
- Traffic shaping

THE MPC826X ATM CONTROLLER

- Utopia 2 hardware interface : multi-PHY control
- APC unit : schedule tables, GCRA algorithm for VBR traffic
- VCI/VPI of incoming cells lookup
- Performance monitoring
- ATM controller parameter RAM description
- RxBD and TxBD format according to the adaptation layer
- Interrupts queue

Renseignements pratiques

Renseignements : 5 jours