



FF4 - MCF548x implementation

This course covers MCF548X ColdFire MCUs, for instance the MCF5485

Objectives

- Optimized code writing based on pipeline knowledge.
- Memory controller understanding, especially DDR SDRAM controller.
- Understanding the operation of the Fast Ethernet controller.
- Detailing the reset sequence.
- Programming of an Interrupt Service Routine.
- Parameterizing the PCI bridge to perform inbound and outbound transactions.
- This course has been delivered several times to companies developing transportation equipments.

A lot of programming examples have been developed by ACSYS to explain the boot sequence and the operation of complex peripherals, such as Fast Ethernet.

-They have been developed with CodeWarrior compiler and are executed under CodeWarrior debugger.

A more detailed course description is available on request at info@ac6-training.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.

Related courses

- Ethernet and switching, reference [N1](#)
- PCI 3.0, reference [IC1](#)
- USB 2.0, reference [IP2](#)
- CAN bus, reference [IA1](#)

Plan

INTRODUCTION TO THE MCF548X FAMILY

Overview

- ColdFire core versions
- Architecture of a typical 548X board
- Mapping of internal resources

CORE ARCHITECTURE

THE V4e COLDFIRE CORE

- Pipeline basics
- Description of assembly instructions
- Floating Point Unit description
- Mac instructions, implementation of a fixed point DFT
- ColdFire instruction set architecture enhancements
- Stack management, subroutine call and return
- C to assembly interface, organization of the stack frame
- Position dependent code vs position independent code
- Section definition
- Exception management : vector table, priority, masking, precise faults
- Memory Management Unit : translation and access control, process protection
- TLB initialization
- Cache basics
- 32-kB cache data and instruction, a four-way set associative organization
- Cache coherency and invalidation, software control
- Internal 32-kB SRAM, initialization code
- Power management

DEBUG FACILITIES

- Intrusive vs non-intrusive debug
- BDM port
- Hardware breakpoints
- Trace port

PLATFORM

RESET

- Reset sources
- Clocking, system clock generation, PLL control, loss of clock detection
- Reset control flow
- Requirements of the boot routine

SIU & INTERRUPT CONTROLLER

- System Control Module
- Internal bus arbitration
- The interrupt controllers : vectorized vs auto-vectorized mode, edge Port Module

HARDWARE IMPLEMENTATION

- Electrical specification, supply voltage sequencing
- Flexbus
- DDR SDRAM basics
- DDR SDRAM Controller
- PCI Controller
- Error management

TIMERS

- Programmable Interrupt Timer Modules
- General Purpose Timer Modules
- Input capture capability

THE MULTI CHANNEL DMA CONTROLLER

- DMA task memory
- DMA sources
- Transfer control descriptors

INTEGRATED I/Os**COMMUNICATION CONTROLLERS**

- The PSC Module
- The DSPI
- The I2C controller
- The FlexCAN controller
- The Fast Ethernet Controller
- The USB 2.0 device controller

INTEGRATED SECURITY ENGINE

- Crypto-channels
- ARC four execution unit
- Multi-function data packet descriptors

Renseignements pratiques

Durée : 4 jours
Prix : 1950 € HT

