



AT2 - AT91SAM9 microcontroller implementation

This course covers AT91SAM9 ARM-based MCU family

Objectives

- The course details the hardware implementation of the AT91SAM9 MCUS.
- The ARM926EJ-S operation is detailed, particularly cache and MMU.
- The boot sequence and the clocking are explained.
- Practical labs on integrated peripherals are based on I/O functions provided by Atmel.
- The course provides examples of internal peripheral software drivers.
- Note that ACSYS does not sell emulation probes and IDEs. Consequently this course has not been designed to convince attendees to buy a particular IDE. The unique objective consists in providing sufficient knowledge to attendees so that they can successfully design a system based on AT91SAM9.
- This course has been delivered several times to companies developing embedded systems, such as medical equipments.
- Note that an additional day on Linux porting onto an AT91SAM9 board may be appended.

A lot of programming examples have been developed by ACSYS to explain the boot sequence, the vector table and the operation of embedded peripherals.

-They have been developed with 2 different IDEs : Keil and IAR.

-Consequently for on site course, it is up to the customer to select the IDE under which labs will be run.

A more detailed course description is available on request at info@ac6-training.com

Prerequisites and related courses

- This course provides an overview of the ARM926 core. Our course reference [R1](#) details the operation of this core.
- The following courses could be of interest:
 - USB Full Speed High Speed and USB On-The-Go, reference [IP2](#)
 - Ethernet and switching, reference [N1](#)
 - CAN bus, reference [IA1](#)

Plan

INTRODUCTION TO AT91SAM9 MCUs

Overview

- ARM core based architecture, AMBA buses
- Multi-layer AHB bus matrix

- The main three blocks : platform, core and input / output peripherals

THE PROCESSOR CORE

THE ARM926EJ-S CORE

- Operating modes : user, system, super, IRQ, FIQ, undef and abort
- ALU data path
- ARM vs Thumb instruction sets, interworking
- Access to memory-mapped locations, addressing modes
- Stack management
- Benefits of condition set capability in ARM state
- C-to-Assembly interface
- Exception mechanism, handler table
- MMU
- Cache operation
- JTAG interface
- Debug facilities

PLATFORM

INFRASTRUCTURE

- Power supplies, internal regulator
- Power-on sequence
- Clock generator, on-chip oscillator, PLL
- Reset controller
- Boot program
- Memory controller
- Internal high-speed flash
- External Bus Interface, SDRAM controller, NAND flash controller
- Power management controller
- Advanced interrupt controller
- External interrupt sources and fast interrupt source
- Parallel input / output controller
- Peripheral DMA controller

INTEGRATED I/Os

TIMERS

- Periodic Interval Timer
- Windowed Watchdog
- Real-time timer
- 3-channel timer / counter

ANALOG-TO-DIGITAL CONVERTER

- Successive Approximation Register 10-bit ADC
- Detail of the analog part, timings
- Conversion triggers

COMMUNICATION CONTROLLERS

- 2-wire interface
 - I2C protocol basics
 - Slave mode vs master mode
 - Transmit and receive sequences
- SPI
 - SPI protocol basics
 - Master / slave operation
 - Transfer sequence
- USART
 - Individual baud rate generators
 - RS485 support
 - Flow control
- Synchronous Serial Controller
 - Independent clock and frame sync signals for each receiver and transmitter
 - I2S analog interface support
 - Time Division Multiplexed support
- Ethernet MAC
 - Accessing PHY registers, auto-negotiation
 - Receive and Transmit buffer management, buffer descriptors
 - Incoming frame filtering
 - Error management
- USB device
 - Full speed operation
 - High Speed device port on AT91SAM9RL64
 - Connection of an external PHY using UTMI+
 - Endpoint configuration
- USB host
 - Overview of the OHCI specification
 - Clarifying the boundary between software and hardware
- Multimedia Card Interface (on demand)
 - MMC and SD card basics
 - Command / response protocol
 - Read sequence
 - Write sequence
- AC97 controller (Specific to AT91SAM9RL64, on demand)
 - Sound encoding
 - Connecting an external audio codec
 - Time slot assigner operation

IMAGE SENSOR INTERFACE

- Connecting an external image sensor
- CCIR656 specification
- Scaling, decimation
- Color space conversion
- FIFO and DMA transfer

LCD CONTROLLER

- Single and Dual scan color and monochrome passive STN LCD panels
- Single scan active TFT LCD panels
- Pixel encoding
- Supported resolution

TOUCH SCREEN ANALOG-TO-DIGITAL CONVERTER

- 6-channel ADC
- Multiple trigger sources
- Conversion sequencer

Renseignements pratiques

Duration : 4 days
Cost : 1500 € HT



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