



NP2 - LPC17xx microcontroller implementation

This course covers NXP Cortex-M3-based LPC17XX MCU family.

Objectives

- This course has 5 main objectives:
 - Describing the hardware implementation and highlighting the pitfalls
 - Describing the ARM Cortex-M3 core architecture
 - Becoming familiar with the IDE and low level programming
 - Describing the units which are interconnected to other modules, such as clocking, interrupt controller and DMA controller, because the boot program generally has to modify the setting of these units
 - Describing independent I/O modules and their drivers.
- Note that this course has been designed from the architecture of the most complex LPC17XX device, the LPC1769.
- Consequently, a chapter has been designed by Acsys for each possible integrated IP.
 - According to the actual reference chosen by the customer, some chapters may be removed.
- Products and services offered by ACSYS:
 - ACSYS is able to assist the customer by providing consultancies. Typical expertises are done during board bringup, hardware schematics review, software debugging, performance tuning.
 - ACSYS has also an expertise in FreeRTOS porting and uIP /LWIP stack or Interniche stack integration.

A lot of programming examples have been developed by ACSYS to help the attendee to become familiar with the IDE he has chosen.

That is why the labs included in this course can be compiled and executed under 3 possible IDEs: IAR, Keil and GCC / Lauterbach Trace32.

A more detailed course description is available on request at info@ac6-training.com

This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Prerequisites and related courses

- This course provides an overview of the ARM Cortex-M3 core. Our course reference [RM2](#) details the operation of this core.
- The following courses could be of interest:
 - USB Full Speed High Speed and USB On-The-Go, reference [IP2](#)
 - Ethernet and switching, reference [N1](#)
 - CAN bus, reference [IA1](#)

Plan

ARCHITECTURE OF LPC17XX MCUs

- ARM core based architecture
- Description of LPC17XX and LPC13XX SoC architecture
- Clarifying the internal data and instruction paths: AHB-lite interconnect, peripheral buses, AHB-to-APB bridges
- Integrated memories
- SoC mapping

THE ARM CORTEX-M3 CORE

- V7-M core family
- Core architecture
- Programming
- Exception behavior, exception return
- Basic interrupt operation, micro-coded interrupt mechanism
- Wakeup Interrupt Controller
- Memory Protection Unit

BECOMING FAMILIAR WITH THE IDE

- Acscs covers 3 IDEs: Keil, IAR and GCC / Lauterbach.
- Thus the customer has just to indicate which one he has chosen
 - Getting started with the IDE
 - Creating a project from scratch
 - C start program

PROGRAMMING AND DEBUGGING

- Debug interface
- Programming

RESET, POWER AND CLOCKING

- Power control
- Reset
- Clocking
- Low power modes

INTERNAL INTERCONNECT

- AHB multi-layer matrix
- DMA

HARDWARE IMPLEMENTATION

- Power pins
- Pinout
- GPIO module
- External Interrupts

INTEGRATED MEMORIES

- Embedded flash memory
- On-chip static SRAM

TIMERS

- Timers 0, 1, 2 and 3
- PWM
- Motor Control PWM
- Quadrature Encoder Interface
- Real Time Clock and backup registers
- Watchdog timer

ANALOG MODULES

- 12-bit Analog-to-Digital Converter
- 10-bit Digital-to-Analog Converter

CONNECTIVITY AND COMMUNICATION

- SPI
- SSP interfaces
- I2S interface
- UART
- I2C
- CAN controllers
- USB FS
- Fast ethernet

Renseignements pratiques

Duration : 5 days
Cost : 1950 € HT



SARL au capital de 15400€ - SIRET 449 597 103 00026 - RCS Nanterre - NAF 722C - Centre de Formation : 19, rue Pierre Curie - 92400 Courbevoie
Siège social et administration : 21, rue Pierre Curie - 92400 Courbevoie - Tél. 01 41 16 80 10 - Fax. 01 41 16 07 78

Last site update: Tue 22 May 2012 10:50:29 AM CEST

<http://www.ac6-formation.com/>