



## FD2 - DSP563XX implementation

This course covers the 563XX 24-bit DSP Freescale family

### Objectives

- The course explains how to design a 56L307 based board
- Optimized coding examples are described
- A generic interrupt handler is introduced
- DMA channels are viewed in detail
- The course focuses on the serial ports SCI and ESSI
- Practical exercises are executed on a 56L307 board

*A lot of programming examples have been developed by ACSYS to explain how to write optimized code. -They have been developed with CodeWarrior compiler and are executed under CodeWarrior debugger.*

*A more detailed course description is available on request at [info@ac6-training.com](mailto:info@ac6-training.com)*

### Prerequisites

- Basic knowledge of signal processing.

### Plan

#### INTRODUCTION TO DIGITAL SIGNAL PROCESSING

- Arithmetic processing of real-time signals
- Modified dual Harvard architecture : the X-memory and the Y-memory
- MAC operation
- DSP 563XX family introduction

#### 563XX ARCHITECTURE

- Core buses
- Processing states
- Reset
- 56L307 mapping

#### THE DSP CORE

- The Data ALU
- The Address Generation Unit
- The Program Control Unit

- The instruction set
- C-to-assembly interface
- The PLL
- The 563XX instruction cache
- Exception management
- The debugging support
- JTAG use to access the OnCE

## **HARDWARE IMPLEMENTATION**

- External memory addressing
- Arbitration protocol
- SRAM interface
- DRAM basics
- DRAM interface

## **THE DMA CONTROLLER**

- Overlap between DMA channel and core
- Channel priority
- Triggering modes
- Circular buffer management

## **THE HOST INTERFACE**

- Host interface description
- Transfer modes
- Handshaking protocols
- DMA access to HTX and HRX data registers
- Boot up using the HIO8 host port
- Programming model : host-side and DSP-side register banks

## **THE TRIPLE TIMER MODULE**

- Timer related pins
- Triple timer modes
- Event capture
- Signal width / period measuring
- PWM
- Watchdog modes

## **THE ENHANCED SYNCHRONOUS SERIAL INTERFACE**

- ESSI signals
- Network mode
- On-Demand mode
- ESSI exceptions
- Transmit and receive sequences

## **THE SERIAL COMMUNICATION INTERFACE**

- SCI block diagram
- Asynchronous vs synchronous operation modes
- Baud rate selection
- Bootstrap loading from the SCI
- Asynchronous transmit and receive sequences

## THE ENHANCED FILTER COPROCESSOR

- PMB interface, FMAC unit, FDM bank, FCM bank
- FIR filter options
- IIR filter options
- Multichannel mode
- Input scaling

## Renseignements pratiques

**Duration : 3 days**  
**Cost : 1650 € HT**



SARL au capital de 15400€ - SIRET 449 597 103 00026 - RCS Nanterre - NAF 722C - Centre de Formation : 19, rue Pierre Curie - 92400 Courbevoie  
Siège social et administration : 21, rue Pierre Curie - 92400 Courbevoie - Tél. 01 41 16 80 10 - Fax. 01 41 16 07 78

Last site update: Mon 13 Feb 2012 02:28:18 PM CET

<http://www.ac6-formation.com/>